

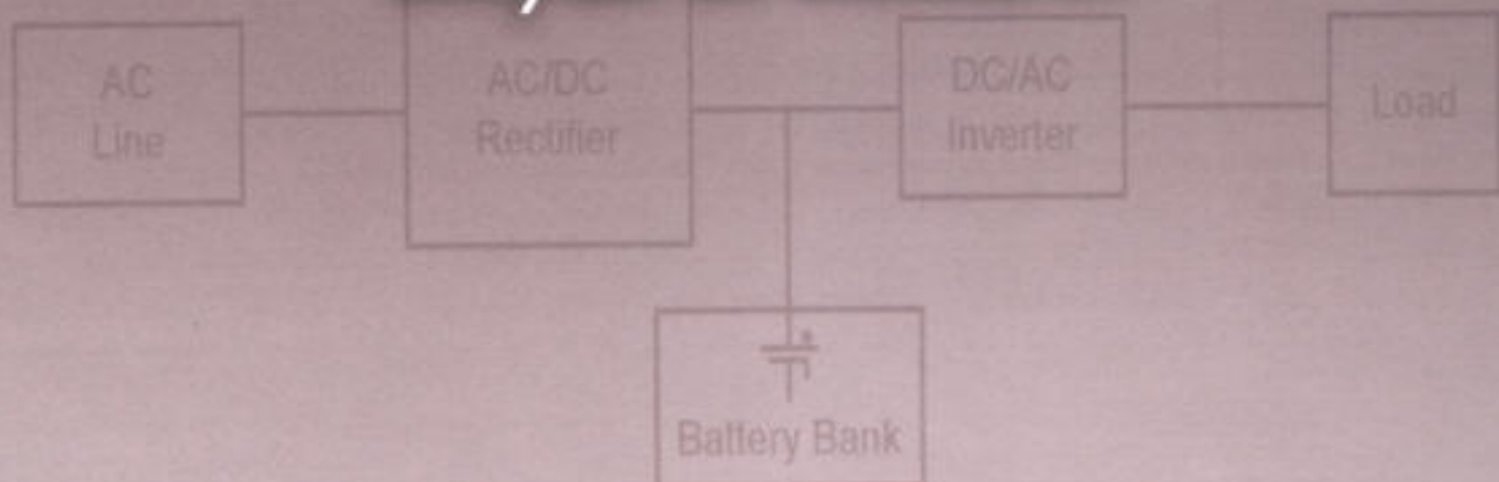
UNINTERRUPTIBLE POWER SUPPLIES AND ACTIVE FILTERS

A detailed circuit diagram of an active power filter system. It shows an AC source connected to a diode bridge rectifier (S1, S2) and a DC link with an inductor (L1). A static switch (S3) and a bypass capacitor (C1) are also shown. The system is connected to a load (Lo) and a battery bank for energy storage. Various components like diodes (D1, D2), capacitors (C1, C2), and inductors (L1, L2) are labeled.

Ali Emadi

Abdolhosein Nasiri

Stoyan B. Bekiarov



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Uninterruptible Power Supplies and Active Filters

Ali Emadi, Abdolhosein Nasiri, and Stoyan B. Bekiarov

UNINTERRUPTIBLE POWER SUPPLIES AND ACTIVE FILTERS

Ali Emadi
Abdolhosein Nasiri
Stoyan B. Bekiarov

Illinois Institute of Technology
Electrical and Computer Engineering Department
Chicago, IL



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To our families

Preface

In recent years, with the increase of nonlinear loads drawing nonsinusoidal currents, power quality distortion has become a serious problem in electrical power systems. Active filters have been known as an effective tool for harmonic mitigation as well as reactive power compensation, load balancing, voltage regulation, and voltage flicker compensation. On the other hand, uninterruptible power supply (UPS) systems provide uninterrupted, reliable, and high-quality power for vital loads. They, in fact, protect sensitive loads against power outages as well as overvoltage and undervoltage conditions. UPS systems also suppress line transients and harmonic disturbances. Applications of UPS systems include medical facilities, life-supporting systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and on-line management systems. Generally, an ideal UPS should be able to deliver uninterrupted power and, simultaneously, provide the necessary power conditioning for the particular power application.

This book describes harmonic-producing loads, effects of harmonics, and harmonic mitigation methods using active filters. Different topologies of active filters and UPS systems, their applications, configurations, control methods, modeling and analysis, and stability issues are also comprehensively discussed.

Recent advancements in the area of power electronics have resulted in a great variety of new topologies and control strategies for active filters and UPS systems. The research has been focused mainly on improving the performance and expanding application areas of these systems. The issue of cost reduction has been attracting the attention of researchers. Reducing the number of switches allows one of the most significant cost reductions. A different technique is replacing controlled switches such as IGBTs, MOSFETs, and thyristors with diodes. Another approach for reducing cost is to develop topologies that employ switches with lower reverse voltage stresses and lower current ratings. This book addresses these new trends in detail.

Ali Emadi

Abdolhosein Nasiri

Stoyan B. Bekiarov

Biography

Ali Emadi received the B.S. and M.S. degrees in electrical engineering with highest distinction from Sharif University of Technology, Tehran, Iran. He also received his Ph.D. degree in electrical engineering specializing in power electronics and motor drives from Texas A&M University, College Station, TX, where he was awarded the Electric Power and Power Electronics Institute (EPPEI) fellowship for his graduate studies. In 1997, he was a lecturer at the Electrical Engineering Department of Sharif University of Technology. Dr. Emadi joined the Electrical and Computer Engineering (ECE) Department of Illinois Institute of Technology (IIT) in August 2000.

Dr. Emadi is the director of Grainger Power Electronics and Motor Drives Laboratories at IIT, where he has established research and teaching laboratories as well as courses in power electronics, motor drives, and vehicular power systems. He is also the co-founder and co-director of IIT Consortium on Advanced Automotive Systems (ICAAS). His main research interests include modeling, analysis, design, and control of power electronic converters/systems and motor drives. His areas of interest also include integrated converters, vehicular power systems, and hybrid electric and fuel cell vehicles.

Dr. Emadi has been named the Eta Kappa Nu Outstanding Young Electrical Engineer for 2003 by virtue of his outstanding contributions to hybrid electric vehicle conversion, for excellence in teaching, and for his involvement in student activities by the Eta Kappa Nu Association, the Electrical Engineering Honor Society. Dr. Emadi is also the recipient of the 2002 University Excellence in Teaching Award from IIT as well as Overall Excellence in Research Award from Office of the President, IIT, for mentoring undergraduate students. He directed a team of students to design and build a novel low-cost brushless DC motor drive for residential applications, which won the First Place Overall Award of the 2003 IEEE/DOE/DOD International Future Energy Challenge for Motor Competition. He is an Associate Editor of IEEE Transactions on Power Electronics and a member of the editorial board of the Journal of Electric Power Components and Systems, the international program committee of Power Generation and Renewable Energy Sources Symposium, the vehicle power and propulsion committee in Vehicular Technology Society of IEEE, and the organizing committee of the Annual Conference on Properties and Applications of Magnetic Materials. Dr. Emadi is the author of more than 130 journal and conference papers as well as three books including *Vehicular Electric Power Systems: Land, Sea, Air, and Space Vehicles* (New York: Marcel Dekker, 2003), *Energy Efficient Electric Motors: Selection and Applications* (New York: Marcel Dekker, 2004), and *Uninterruptible Power Supplies and*

Active Filters (Boca Raton: CRC Press, 2004). He is also the co-author of *Modern Electric, Hybrid Electric, and Fuel Cell Vehicles: Fundamentals, Theory, and Design* (Boca Raton: CRC Press, 2004). Dr. Emadi is also the editor of the *Handbook of Automotive Power Electronics and Motor Drives* (New York: Marcel Dekker, 2005). He is a senior member of IEEE and a member of SAE. He is also listed in the International *Who's Who of Professionals* and *Who's Who in Engineering Academia*.

Abdolhosein Nasiri received the B.S. and M.S. degrees in electrical engineering with distinct honor from Sharif University of Technology, Tehran, Iran. He also received his Ph.D. degree in electrical engineering specializing in power electronics and motor drives from Illinois Institute of Technology, Chicago, Illinois. He was listed in the *Who's Who* among students in American Universities and Colleges. He joined Baxter Healthcare Corporation in Deerfield, Illinois, as R&D electrical engineer in 2003 and, currently, he is working for ForHealth Technologies in Daytona Beach, Florida, as a senior electrical engineer. Dr. Nasiri has 15 journal and conference papers and is a reviewer of IEEE journal and conference papers. His Ph.D. dissertation was focused on configurations, modeling, and digital control of series-parallel active filter/UPS systems. His areas of interest include power electronic converters, integrated power converters, active filter and UPS systems, switching power supplies, and adjustable speed drives.

Stoyan B. Bekiarov received his M.S. degree in electrical engineering in 1994 from Technical University-Sofia, Bulgaria. From 1994 to 2000, he was employed by the Grovet-LTD, Bulgaria, as a Project Engineer. He received his Ph.D. degree in electrical engineering specializing in power electronics and motor drives from Illinois Institute of Technology, Chicago, Illinois, in 2004. Dr. Bekiarov is currently a Senior Engineer at C.E. Niehoff & Co. His interests include design and control of power electronic converters and systems, electric power management systems, and brushless alternators for military and heavy-duty automotive systems.

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1

Uninterruptible Power Supplies

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Uninterruptible power supply (UPS) systems provide uninterrupted, reliable, and high-quality power for vital loads. They, in fact, protect sensitive loads against power outages as well as overvoltage and undervoltage conditions. UPS systems also suppress line transients and harmonic disturbances. Applications of UPS systems include medical facilities, life-support systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and on-line management systems.

Generally, an ideal UPS should be able to deliver uninterrupted power while simultaneously providing the necessary power conditioning for the particular power application. Therefore, an ideal UPS should have the following features [1]:

- Regulated sinusoidal output voltage with low total harmonic distortion (THD) independent of the changes in the input voltage or in the load, linear or nonlinear, balanced or unbalanced.
- On-line operation, which means zero switching time from normal to backup mode and vice versa.
- Low THD sinusoidal input current and unity power factor.
- High reliability.
- Bypass as a redundant source of power in the case of internal failure.
- High efficiency.
- Low electromagnetic interference (EMI) and acoustic noise.
- Electric isolation of the battery, output, and input.
- Low maintenance.
- Low cost, weight, and size.

The advances in power electronics during the past three decades have resulted in a great variety of new topologies and control strategies for UPS systems. The research has been focused mainly on improving performance and expanding application areas of UPS systems. The issue of reducing the cost of converters has recently attracted the attention of researchers [2–15]. Reducing the number of switches provides the most significant cost reduction. Another form of cost reduction is to replace active switches such as IGBTs, MOSFETs, and thyristors with diodes. Not only are diodes more reasonable than the controlled switches, but there is also a cost reduction from eliminating gate drivers for active switches and power supplies for gate drivers.

Another way of reducing cost is to develop topologies that employ switches with lower reverse voltage stresses and lower current ratings, which means less silicon and smaller switching losses resulting in lower cost and higher efficiency.

1.1 Classification

UPS systems are classified into three general types: static, rotary, and hybrid static/rotary. In this section, we explain these three categories of the UPS systems.

1.1.1 Static UPS

Static UPS systems are the most commonly used UPS systems. They have a broad variety of applications from low-power personal computers and telecommunication systems, to medium-power medical systems, and to high-power utility systems. Their main advantages are high efficiency, high

reliability, and low THD. The inherent problems related to static UPS systems are poor performance with nonlinear and unbalanced loads and high cost for achieving very high reliability. On-line, off-line, and line-interactive configurations are the main types of the static UPS systems [2, 14, 15].

1.1.1.1 On-Line UPS

On-line UPS systems appeared during the 1970s [14]. They consist of a rectifier/charger, a battery set, an inverter, and a static switch (bypass). Other names for this configuration are inverter-preferred UPS and double-conversion UPS [14, 15]. Figure 1.1 shows the block diagram of a typical on-line UPS. The rectifier/charger continuously supplies the DC bus with power. Its power rating is required to meet 100% of the power demanded by the load as well as the power demanded for charging the battery bank. The batteries are usually sealed lead-acid type. They are rated in order to supply power during the backup time, when the AC line is not available. The duration of this time varies in different applications. The inverter is rated at 100% of the load power since it must supply the load during the normal mode of operation as well as during the backup time. It is always on; hence, there is no transfer time associated with the transition from normal mode to stored energy mode. This is the main advantage of the on-line UPS systems. The static switch provides redundancy of the power source in the case of UPS malfunction or overloading. The AC line and load voltage must be in phase in order to use the static switch. This can be achieved easily by locked-phase control loop.

There are three operating modes related to this topology: normal mode, stored energy mode, and bypass mode.

1.1.1.1.1 Normal Mode of Operation

During this mode of operation, the power to the load is continuously supplied via the rectifier/charger and inverter. In fact, a double conversion, that is, AC/DC and DC/AC, takes place. It allows very good line conditioning. The AC/DC converter charges the battery set and supplies power to the load via the inverter. Therefore, it has the highest power rating in this topology, increasing the cost.

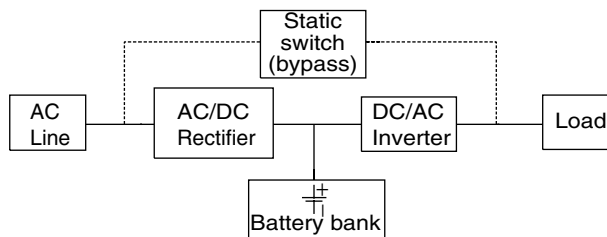


FIGURE 1.1

Block diagram of a typical on-line UPS system.

1.1.1.1.2 *Stored-Energy Mode of Operation*

When the AC input voltage is outside the preset tolerance, the inverter and battery maintain continuity of power to the load. The duration of this mode is the duration of the preset UPS backup time or until the AC line returns within the preset tolerance. When the AC line returns, a phase-locked loop (PLL) makes the load voltage in phase with the input voltage and after that the UPS system returns to the normal operating mode.

1.1.1.1.3 *Bypass Mode of Operation*

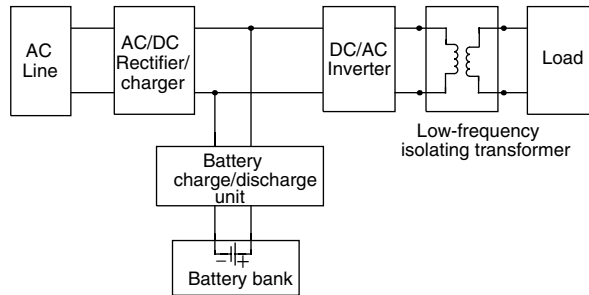
The UPS operates in this mode in case of an internal malfunction such as overcurrent. This mode is also used for fault clearing. It should be mentioned that the output frequency should be the same as the AC line frequency in order to ensure the transfer of power. In some cases, there can be a maintenance bypass as well. A manual switch usually operates it.

The main advantages of on-line UPS are very wide tolerance to the input voltage variation and very precise regulation of output voltage. In addition, there is no transfer time during the transition from normal to stored energy mode. It is also possible to regulate or change the output frequency [14].

The main disadvantages of this topology are low-power factor, high THD at the input, and low efficiency. The input current is distorted by the rectifier unless an extra power factor correction (PFC) circuit is added; but, this adds to the cost of the UPS system [2]. Because of this inherently low input power factor, the on-line UPS cannot efficiently utilize the utility network and local installation. The low efficiency is inherent to this topology because of the double-conversion nature of this UPS. Power flow through the rectifier and inverter during the normal operation means higher power losses and lower efficiency compared to off-line and line-interactive UPS systems.

Despite the disadvantages, double-conversion UPS is the most preferred topology in performance, power conditioning, and load protection. This is the reason why they have a very broad range of applications from a few kVA to several MVA. This broad range of applications brings a large diversity of topologies in on-line UPS systems [3]. Each topology tries to solve different specific problems and the particular choice depends upon the particular application. However, generally, there are two major types of double-conversion topologies: with a low-frequency transformer isolation and with a high-frequency transformer isolation. [Figure 1.2](#) shows the block diagram of an on-line UPS with a low-frequency transformer isolation at the output.

In this configuration, there is an isolating transformer at the output, which operates at low frequency. This, of course, means a larger transformer. Therefore, this topology is used only in high-power ratings (>20 kVA), where the switching frequency is limited to less than 2 kHz. Apart from the large size of the isolating transformer, the drawback of this topology is high acoustic noise from the transformer as well as the reactor of the output filter [3]. This topology also has a poor transient response to the changes in the load and input voltage.

**FIGURE 1.2**

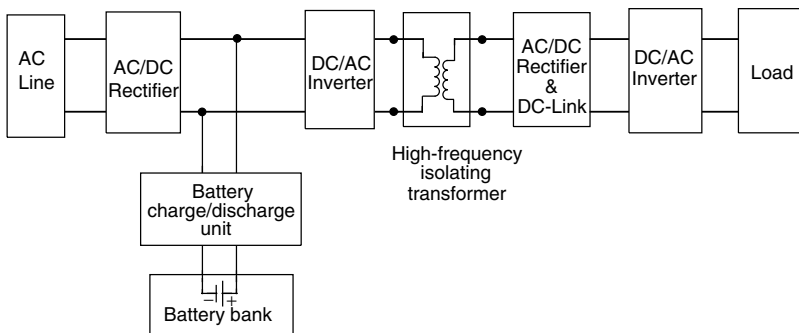
Block diagram of an on-line UPS with a low-frequency transformer isolation at the output.

By increasing the switching frequency of the inverter above 20 kHz, these problems are solved, except for the size of the isolating transformer, since it is independent of the switching frequency. A topology employing a high-frequency transformer link can significantly reduce the weight and the size of the transformer [3, 16]. The use of high-frequency pulse width modulation (PWM) techniques can additionally reduce the size of the output filter. Figure 1.3 shows the block diagram of an on-line UPS with a high-frequency transformer isolation between the input and the output.

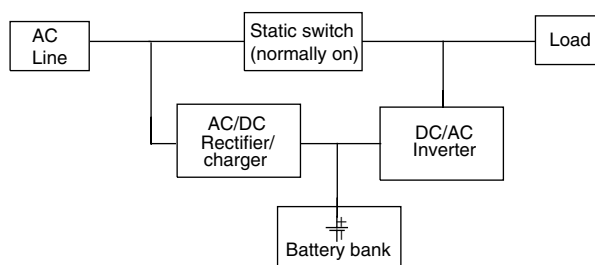
In contrast with the on-line UPS, which drives the load in the normal operating mode, off-line UPS provides power for the load in case of power outage, overvoltage, and undervoltage situations in the AC line.

1.1.1.2 Off-Line UPS

This configuration is also known as the standby UPS or line-preferred UPS [14, 15]. As shown in Figure 1.4, it consists of an AC/DC converter, a battery bank, a DC/AC inverter, and a static switch. A filter may be used at the output of the UPS or inverter to improve the quality of the output voltage. The static switch is on during the normal mode of operation when the AC line is alive. Therefore,

**FIGURE 1.3**

Block diagram of an on-line UPS with high-frequency transformer isolation.

**FIGURE 1.4**

Block diagram of a typical off-line UPS system.

the load is supplied with power from the AC line directly without any power conditioning. The AC/DC converter charges the battery set. It is rated at a much lower power rating than the rectifier/charger in an on-line UPS since it is not required to meet the power demand of the load. This, in turn, makes the off-line UPS systems more reasonable than the on-line UPS systems. The inverter is rated at 100% of the load's demand. It is connected in parallel to the load and stays standby during the normal mode of operation. It is turned on only when the primary power is out of a given preset tolerance or is not available at all. During this mode of operation, the power to the load is supplied by the battery set via the inverter for the duration of the preset backup time or until the AC line is back again. The duration of the switching time depends on the starting time of the inverter. The transfer time is usually about $\frac{1}{4}$ line cycle, which is enough for most of the applications such as personal computers.

The DC/AC inverter is conventionally off in this mode. Therefore, an off-line UPS is not usually correcting the power factor. However, in the normal mode of operation, the DC/AC inverter may be used as an active filter to reduce the harmonic content of the line current or improve the power factor of the load. Further modification can also be made to reduce the harmonic content of the sinking current by the AC/DC converter when charging the battery. Yet, these increase the complexity of the system.

There are two operating modes for an off-line UPS system: normal mode and stored-energy mode.

1.1.1.2.1 Normal Mode of Operation

In this mode, the AC line supplies the load via filter/conditioner, which, in fact, is not always required, but often exists. The filter/conditioner depends on the requirements of the particular load and the quality of the AC line power supply. The AC/DC converter charges the battery in this mode in order to provide backup power for the stored-energy mode of operation.

1.1.1.2.2 Stored-Energy Mode of Operation

When the AC line is beyond the preset tolerance or is not available, the load is supplied by the battery set through the inverter for the backup time or until the AC line is available again. The rating of the AC/DC converter has to

meet only the charging requirements of the battery, which contributes to the lower cost of this UPS.

The main advantages of this topology are a simple design, low cost, and small size. The line conditioning, when there is such a feature, is passive and the technique is very robust. On the other hand, lack of real isolation of the load from the AC line, no output voltage regulation, long switching time, and poor performance with nonlinear loads are the main disadvantages.

The use of a three-winding transformer, as shown in Figure 1.5, can provide electric isolation for the off-line UPS. This technique has a high reliability at a moderate cost. The transformer allows limited power conditioning for the output voltage as well. The use of a Ferro-resonant transformer leads to a heavier UPS with a lower efficiency [15]. The disadvantages of off-line UPS systems limit their application to less than 2 kVA [3, 14, 15].

1.1.1.3 Line-Interactive UPS

In the 1990s, line-interactive UPS systems were presented [14]. As shown in Figure 1.6, a line-interactive UPS system consists of a static switch, a series inductor, a bidirectional converter, and a battery set.

A line-interactive UPS system can operate either as an on-line UPS or as an off-line UPS. For an off-line line-interactive UPS, the series inductor is not required. However, most of the line-interactive UPS systems operate on-line in order to either improve the power factor of the load or regulate the output voltage for the load.

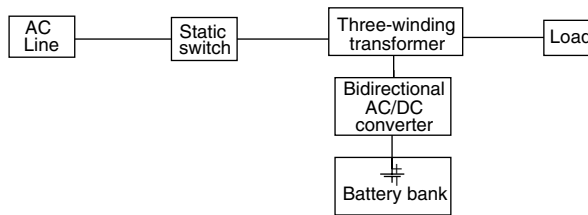


FIGURE 1.5

Block diagram of a typical off-line UPS using a three-winding transformer for electric isolation.

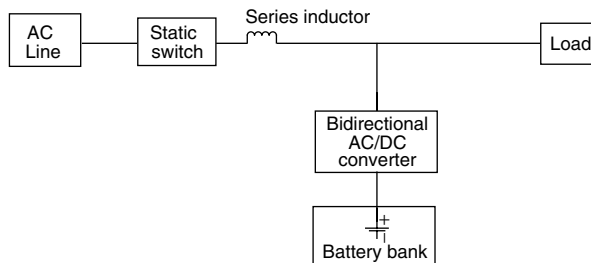


FIGURE 1.6

Block diagram of a typical line-interactive UPS system.

When the AC line is within the preset tolerance, it feeds the load directly. The inverter is connected in parallel with the load and charges the battery. It may also supply the reactive power required to keep the power factor close to unity or to regulate the output voltage [15, 17–20]. As mentioned, this power-conditioning function of the inverter is used only in on-line line-interactive UPS systems. We use the equivalent circuit for the fundamental frequency of a line-interactive UPS system, as shown in Figure 1.7, to explain the power-conditioning function of the inverter.

The amplitude of V_i is determined by the battery voltage and the modulation index m of the PWM converter. Hence, it can be adjusted independent of the AC line voltage. The shift angle δ , between V_1 and V_i , can be varied as well.

We assume that the AC line voltage V_1 is 100% of its nominal, and the output voltage V_i is 100% of its nominal as well. The shift angle δ is determined by the real power demanded by the load.

$$P = \{(V_i V_1) \sin \delta\} / j\omega L \quad (1.1)$$

The series inductor voltage drop is designed to be small under normal rated conditions — usually $\delta \cong 15^\circ$. Hence, the power factor is very close to unity under these conditions: $\cos \phi = \cos (\delta/2)$. The phasor diagram for this case is shown in Figure 1.8.

By assuming a pure resistive load, the inverter supplies only the reactive power necessary to compensate the reactive voltage drop across the series inductor. When the load has a reactive part, the inverter will compensate it

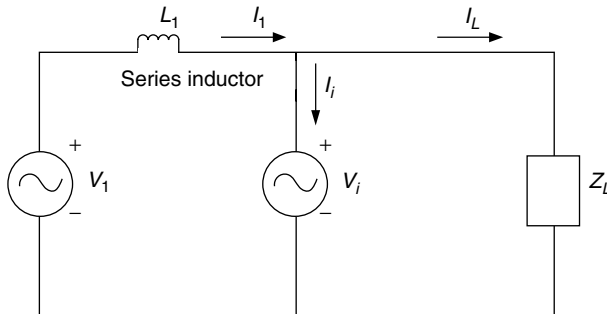


FIGURE 1.7
Equivalent circuit for the fundamental frequency of a line-interactive UPS.

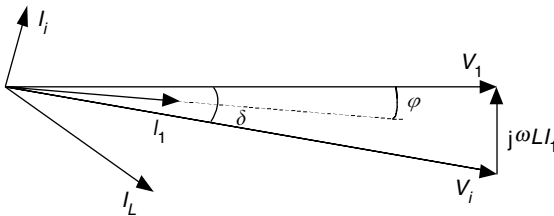


FIGURE 1.8
Phasor diagram for the equivalent circuit of Figure 1.7.

as well. In fact, current drawn from the AC line is always sinusoidal and kept in phase with the AC line voltage.

The principle of the output voltage regulation can be easily understood with the help of the phasor diagrams in Figure 1.9. The inverter supplies reactive power for undervoltage and consumes reactive power for overvoltage situations. Since it is desirable to draw only reactive power from the inverter, it is obvious that the power factor deteriorates when a voltage regulation is implemented. When the AC line is not available or is beyond the preset tolerance, the inverter supplies the load with energy from the battery set. As a result, it is rated to meet 100% of the power demanded by the load and the power demanded for charging the battery set. The static switch is turned off to prevent back feed to the AC line.

There are two operating modes for a line-interactive UPS: normal and stored-energy.

1.1.1.3.1 Normal Mode of Operation

The power flow during this mode is from the AC line to the load. The bidirectional converter plays the role of a charger for the battery set. It can also keep the output voltage relatively stabilized and sinusoidal or improve the power factor of the load with a proper PWM control. The current taken from the AC line is mainly the current for the load. In fact, no additional harmonics are injected from the UPS into the AC line. This is an important advantage compared to the conventional on-line double-conversion UPS.

In order to enable better regulation for the output voltage during this mode, a bulk constant voltage transformer can be added to the output; however, it is heavy, large, and expensive [19].

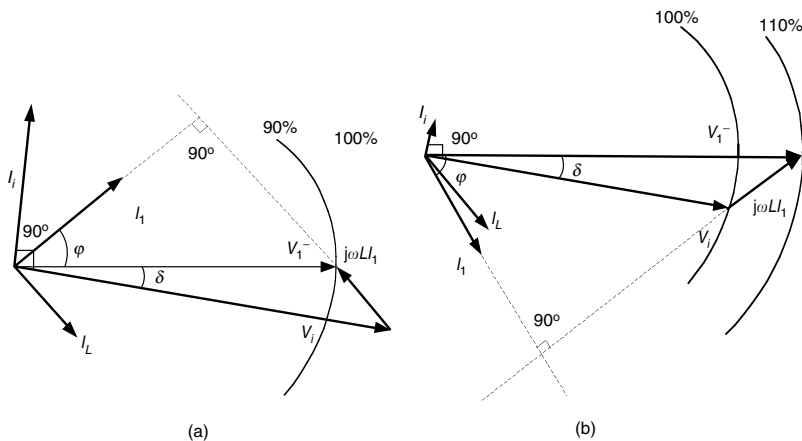


FIGURE 1.9

Phasor diagram for (a) undervoltage and (b) overvoltage situations.

1.1.1.3.2 Stored-Energy Mode of Operation

In this mode, the bidirectional converter operates as an inverter and supplies the load with power from the battery set. The static switch disconnects the AC line in order to prevent back feed from the inverter. The duration of this mode is the duration of the preset backup time or until the AC line returns within the tolerance.

The main advantages of the line-interactive UPS systems are a simple design and, as a result, high reliability and lower cost compared to the on-line UPS systems. They also have good harmonic suppression for the input current. Since this is, in fact, a single-stage conversion topology, the efficiency is higher than that of the double-conversion UPS.

Its main disadvantage is the lack of effective isolation of the load from the AC line. The use of a transformer in the output can eliminate this; but, it will add to the cost, size, and weight of the UPS system. Furthermore, the output voltage conditioning is not good because the inverter is not connected in series with the load. In addition, since the AC line supplies the load directly during the normal mode of operation, there is no possibility for regulation of the output frequency.

The new series-parallel line-interactive topology, called delta-conversion UPS, can simultaneously achieve both unity power factor and precise regulation of the output voltage, which is not possible with a conventional line-interactive UPS. Its configuration is shown in Figure 1.10. It consists of two bidirectional converters connected to a common battery set, static switch, and a series transformer. The series bidirectional converter is rated at 20% of the output power of the UPS and it is connected via a transformer in series with the AC line. The second bidirectional converter is the usual inverter for a line-interactive UPS connected in parallel to the load and rated at 100% of the output power. The parallel converter keeps output voltage stable and precisely regulated by PWM control. The series converter compensates any differences between output and input voltages. It also controls the input power factor to unity and, at the same time, controls the charging of the battery. When the AC line is within the preset tolerance, most of the power is

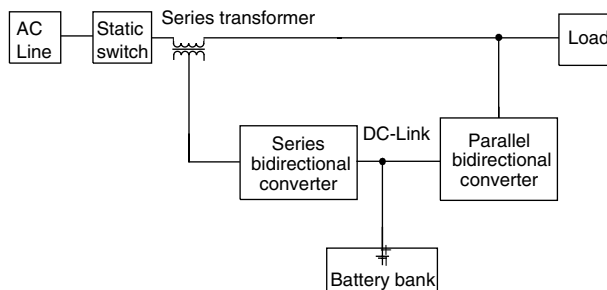


FIGURE 1.10

Block diagram of a typical series-parallel line-interactive (delta-conversion) UPS.

supplied directly from the AC line to the load. Only a small part of the total power, usually up to 15%, flows through the series and parallel converters. This power is needed to compensate for any differences between the input and the output voltages and to make the input power factor unity. Since an important portion of the power (about 85%) flows without any conversion from the AC line to the load, the efficiency of this UPS is relatively high. Therefore, the delta-conversion UPS is used in high-power rating applications, where the efficiency is a key factor. However, the complicated control of this topology limits its applications. Another disadvantage is the lack of electrical isolation of the load from the AC line.

1.1.2 Rotary UPS

A typical rotary UPS is shown in Figure 1.11. It consists of an AC motor, a DC machine, an AC generator, and a battery bank. Electric machines are mechanically coupled. There are two operating modes: normal and stored energy. During the normal mode of operation, the AC line supplies the AC motor, which drives the DC machine. The DC machine drives the AC generator, which supplies the load. During the stored energy mode of operation, the battery bank supplies the DC machine, which in turn drives the AC generator. The AC generator supplies the load.

The rotary UPS systems are more reliable than the static UPS systems. However, they require more maintenance and have a much larger size and weight. But, they have many advantages making them desirable in high-power applications. One of the advantages of the rotary UPS systems is that the transient overload capability is 300 to 600% of the full load for rapid fault clearing. The transient overload capability for the static UPS systems is typically 150% for a short term. The performance of the rotary UPS systems with nonlinear loads is good because of the low output impedance. The input current THD is very low, typically 3% or less. The electromagnetic interference (EMI) is also low. The efficiency is usually 85% or higher [21, 22].

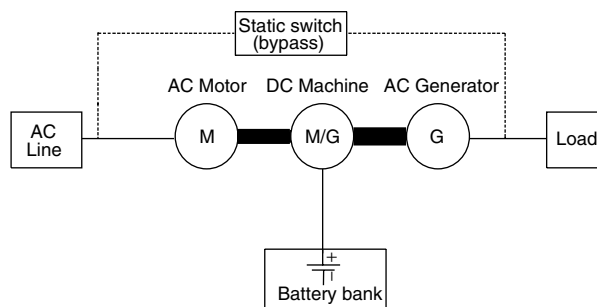


FIGURE 1.11

Block diagram of a typical rotary UPS system.

1.1.3 Hybrid Static/Rotary UPS

Hybrid static/rotary UPS systems combine the main features of both static and rotary UPS systems. They have low output impedance, high reliability, excellent frequency stability, and low maintenance cost. These are because of the missing mechanical commutator [21, 22]. In Figure 1.12, a typical hybrid static/rotary UPS is depicted. It consists of a bidirectional AC/DC converter, an AC motor, an AC generator, a battery bank, and a static switch.

During the normal mode of operation, the AC motor is fed from the AC line and drives the generator. The AC generator supplies the load. The bidirectional converter, which behaves as a rectifier, charges the battery.

During the stored-energy mode of operation, the inverter supplies the AC generator from the battery set through the AC motor. In fact, the bidirectional converter, which behaves as an inverter, drives the AC motor. The AC motor drives the generator supplying the load. When an internal malfunction in the UPS system occurs, the static switch (bypass) is turned on and the load is supplied directly from the AC line. However, since the AC line and output voltage are not synchronized, the transition is not transient-free.

The AC generator is started on utility power to avoid starting current overloads allowing the inverter to be rated for the normal operation. After the AC generator is on, the AC line is disconnected and the supply to the AC generator is given by the inverter. It is relatively easy because of the large inertia of the AC generator. This configuration has the advantage that the transfer from the AC line to the inverter takes place under controlled conditions instead of under fault conditions when different undesired conditions can influence the transfer. Another good point is that the inverter is always on, allowing no transfer time for switching to the stored-energy mode of operation [21].

The main advantages of this UPS over the static UPS include low output impedance, low THD with nonlinear loads, higher reliability, and better isolation. Hybrid UPS systems are usually used in very high-power applications, that is, several hundreds kVA.

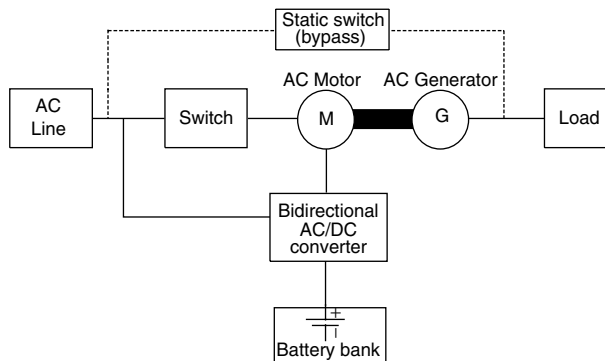


FIGURE 1.12

Block diagram of a typical hybrid static/rotary UPS.

1.2 Batteries for UPS Applications

The most important features of the UPS systems are their reliability and availability. The component that influences this characteristic most considerably is the battery. Batteries must carry the power supply to the load when the AC line fails. If they are not capable of doing this, the whole UPS system fails, regardless of how well designed the power electronic circuit is. In addition, batteries usually determine where the UPS systems will be placed because they require more space and have a weight greater than all the other components of UPS systems. In many cases, batteries constitute considerable parts of the cost of the whole systems.

1.2.1 History

The first UPS systems were employed in large centralized installations to backup critical loads in hospitals and telecommunication offices. Batteries in these large installations were placed in separate, special buildings, which provided ventilation and allowed continuous maintenance. The type of batteries used was flooded lead–acid, which has a long life and excellent long-duration discharge rates, usually 5 to 20 h.

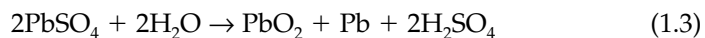
Nowadays, there is another approach for providing backup for critical loads — the distributed approach [23]. Here, smaller UPS systems are used to supply particular small loads. This tendency forced the UPS systems to move from special buildings to offices and hospital rooms. This has led to the requirement for compatibility with the office environmental and no-maintenance requirements. As a result, valve-regulated lead–acid (VRLA) or so-called sealed lead–acid batteries appeared on the market.

1.2.2 Valve-Regulated Lead–Acid Batteries

The basic lead–acid battery is a set of positive and negative electrodes consisting of lead or lead–alloy grids coated with a paste of active material composed of different lead compounds. The positive electrodes are separated from the negative ones by a fiberglass-retaining mat, which usually surrounds the positive plate. The battery is made wet by a sulfuric acid electrolyte solution. The discharge reaction is as follows:



Also, the recharge reaction is the reverse of Equation 1.2:



As a result of recharge, the lead sulfate returns to lead dioxide on the positive plate and sponge lead on the negative plate. The efficiency of the

recharge reaction can be 100%; but it depends on the state of charge (SOC) of the battery. When the efficiency of the reaction is less than 100%, the electrolysis of water occurs. As a result, evolution of hydrogen on the negative plate and oxygen on the positive plate take place.



Charging of batteries above the manufacturer's recommended ratings or charging at these ratings but at higher temperatures causes additional evolution of hydrogen and oxygen. In a flooded electrolyte system, the evolved hydrogen and oxygen are vented out of the cell and the loss of water must be compensated. In VRLA batteries, the compensation of water is impossible. The batteries work on oxygen recombination. The hydrogen evolution is suppressed, and the evolved oxygen is recombined under pressure.

There are two basic types of VRLA batteries: absorbed electrolyte and gelled electrolyte. In the absorbed electrolyte design, the liquid electrolyte is contained in a highly absorbent separator, which isolates the positive plates from the negative plates. This type of battery is designed specifically for UPS applications and is capable of providing a very high short-duration current. The gelled electrolyte VRLA batteries are similar to the flooded design; but the electrolyte is in the form of a gelled mass. In addition, internal pressure is regulated in order to allow oxygen recombination. They can provide a high rate of short-duration currents; but generally, they are more suitable for long discharge applications such as telecommunications [24].

1.2.3 UPS Battery Features

The main requirement for the VRLA batteries designed for UPS applications is to provide a high short-duration current because the duration of the backup time for the UPS systems is usually short — from a few seconds to an hour — usually about 15 min [25]. There are two main differences between the typical VRLA batteries and UPS-designed VRLA batteries. First, in order to provide a higher current for a short time, the UPS-designed batteries need a more active surface area, which is why these batteries have a higher number of thinner plates. The second difference is that the UPS-designed batteries must have a lower internal resistance in order to carry higher currents at lower losses. To achieve this, battery manufacturers remove the fiberglass mat surrounding the positive plate. Instead, they mix active material with integrated fibers. This reduces the battery impedance. Apart from this, designers make the batteries with larger and heavier current conductors in order to carry higher currents.

1.2.4 Problems

Reducing the internal resistance of the batteries also has negative effects. Particularly, two separate problems occur by removing the fiberglass mat.

First, the PbO_2 sedimentation is much higher. Second, the low internal resistance causes problems with the DC and AC ripples of the voltage across the batteries [26]. The DC ripples are the fluctuations in the unsmoothed rectifier output voltage. They increase the internal temperature of the batteries. Although this increment is usually a few degrees Centigrade, it is very harmful for the battery life because each degree Centigrade rise in temperature reduces the battery life by about 10%.

AC ripples are sinusoidal and are superimposed over the DC component. They are also classified as discharge and nondischarge type. When their amplitude is less than the DC component amplitude, as shown in Figure 1.13, the AC ripples are classified as nondischarged. When their amplitude is larger than the DC component amplitude, as shown in Figure 1.14, the AC ripple current becomes both positive and negative, and these AC ripples are classified as discharge AC ripples.

The nondischarge AC ripples have the same effect over the battery as the DC ripples. They increase the internal temperature of the battery. The discharge AC ripples lead to capacity walk-down caused by high-frequency shallow cycling (HFSC). Because the AC ripples are much larger in amplitude than the DC component, they drive the battery into charging and discharging cycles at a rate determined by the frequency of the AC signal. The low-frequency AC ripples are especially harmful for the battery SOC. Assume that we have a fully charged battery installed on a float charging system that has significant AC ripples. The DC float current is set at such a level as to compensate for any self-discharge and to provide some overcharge to keep both plates properly polarized. The superimposed AC discharge ripples drive the battery into charge–discharge cycles. The negative current will discharge the

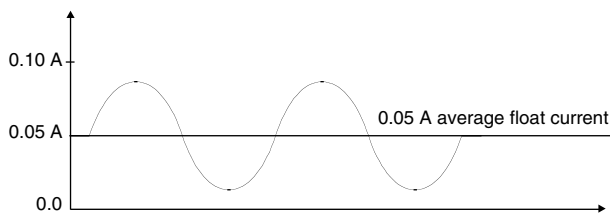


FIGURE 1.13
Nondischarge AC ripple current.

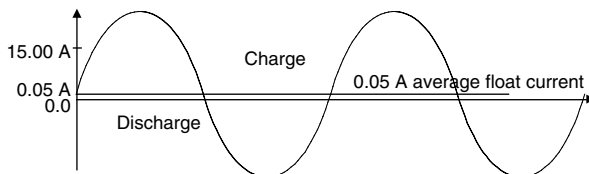


FIGURE 1.14
Discharge AC ripple current.

battery with 100% efficiency. The positive current will charge the battery with an efficiency of about 10%. The remaining 90% of the power will go toward overcharging the battery, resulting in electrolysis of the water and evolution of hydrogen and oxygen. Because of the inequality of the power charged and discharged to the battery over one cycle, after a number of cycles, the battery will experience the so-called capacity walk-down. This process will continue until the battery reaches about 80% of its capacity, where the efficiency of both the charge and discharge processes is 100%. This HFSC causes premature failure of batteries, where the power quality supplied to the battery is poor.

1.2.5 Charging Strategies

Charging strategy for the VRLA UPS-designed batteries is a floating charge, where the battery is continuously connected to a constant current (CC) or a constant voltage (CV). Often, a combination of both is used, as shown in Figure 1.15. During the initial stage of the charging process, when the open-circuit voltage of the battery is low, it is charged at the CC mode. The battery voltage rises slowly in this period. After a certain level of power is absorbed by the battery, its voltage starts to rise quickly and, if not limited, goes into the gassing stage. To avoid this, the battery is switched to the CV charge mode.

However, this float charge method is difficult to perform for two reasons. First, the overvoltage, which is usually about 100 mV above the open-circuit voltage of the battery, is unevenly distributed among the cells in a series string of battery cells. Second, the overvoltage applied has different effects on the positive and negative plates in a single cell. Generally, the applied floating voltage is intended to be high enough to ensure that both the positive and negative plates are significantly polarized and, at the same time, the positive plate is in a region of minimal grid corrosion. Because of the oxygen recombination, the potential of the negative plate decreases and if this oxygen recombination is of a significant amount and the applied float voltage is not large enough, the potential of the negative plate can drop below the open-circuit potential, that is, it goes to the discharge mode. At the same time, because the floating voltage applied to the positive and the negative plates is constant, the potential of the positive plate will increase and eventually can enter the high-corrosion region. We can summarize that, for the common case, when the open-circuit voltage of a cell is 2.17 V at 100% SOC and the overvoltage is 100 mV, the

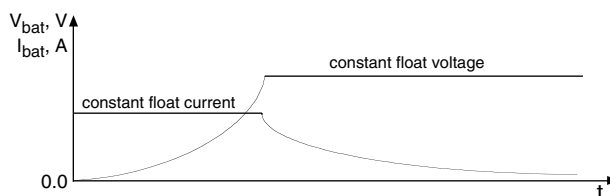


FIGURE 1.15
CC/CV charging method.

applied floating voltage of 2.27 V cannot guarantee that all cells will maintain 100% SOC. If we apply a higher float voltage to ensure that both plates are properly polarized, the positive plate proceeds to the high-corrosion region, and substantial overcharge takes place. The solution is the so-called intermittent charging (IC) method, which was proposed for the first time by Don Reid in 1984. The concept is that the battery is charged with higher than 100 mV overvoltage for a short period of time and, after that, it is off-line for a longer period of time. The gain is that the higher floating voltage ensures that both plates are favorably polarized and, at the same time, the overvoltage is not of a short duration. There are two types of IC methods: time charge, where the battery is charged periodically, for example, 5 min every hour; and trigger voltage charge, where a threshold voltage level triggers the charge process on, and, when 100% SOC is achieved, the process is turned off [27].

1.2.6 Failure Category

Failures in batteries can be categorized into three types resulting in high impedance, low impedance, and deterioration of capacity. Failures resulting in high impedance are caused by the corrosion of plates, loose contact between the active material on plates, or low specific gravity of acid. Failures resulting in low impedance are caused by the short circuit between the plates. Failures resulting in the deterioration of capacity are caused by deep discharge, cycling usage, high temperature, or dryout [28].

1.2.7 Monitoring

Monitoring of flooded batteries is easy to implement. It is based on the cell voltage and level of specific acid gravity and water. Because of the physical constraints, we cannot rely on these parameters for monitoring VRLA batteries. We do not have access to the separate cells in monoblocks of the VRLA battery and to the acid solution inside the battery, which is why the monitoring of VRLA batteries is very difficult to perform, and the results are not very reliable. There are three basic methods for monitoring VRLA batteries: voltage-based, current-based, and impedance-based [28]. In voltage-based methods, lookup tables are used to detect any abnormalities in the discharge mode. In these tables, information about voltage level, as functions of discharge current and time of discharge is stored in computer memory. This information is continuously monitored. There are two problems associated with this method. First, monitoring is possible only during the discharge mode; hence, no information about SOC is available during the float charge. Second, high and low impedance failures can be detected surely by this method, but deterioration of capacity failures cannot be detected, which is why the results from this method may be misinterpreted.

The current-based monitoring method uses a discharge current or a float charging current as an information source. Hence, it is available both in flat

charging and discharging modes. However, the charging current tends to change with aging of the battery. It is also a function of the temperature and applied cell voltage. Therefore, the danger of misinterpretation of the results exists. The third method is the impedance-based method. This approach is based on measurement of the relation between the voltage and current when injecting small AC currents or voltages into the battery. This is the so-called small signal method. Another method is to use large load current step-changes and to measure the relation of the voltage and current. Results from both small and large signal methods are subject to large misinterpretation and, generally, these methods are not reliable. In summary, it can be concluded that, presently, there is no highly reliable method available for monitoring VRLA batteries. This is a large, open field for research since the importance of monitoring is essential to ensuring the reliability and availability of the whole UPS system.

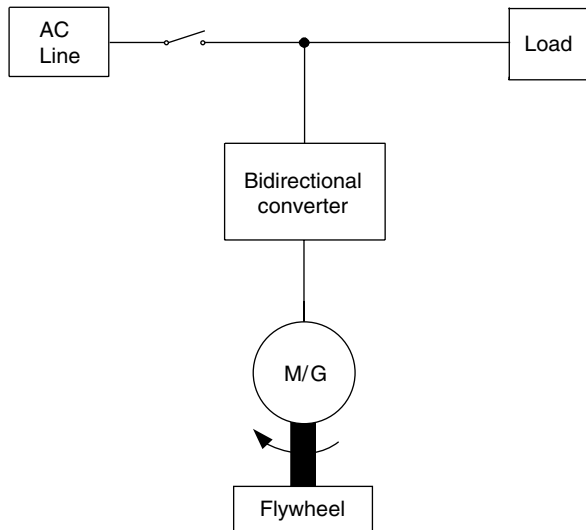
1.3 Flywheels for UPS Applications

Until recently, the only energy-storage technology available was the electrochemical battery, mostly lead-acid batteries. Even though the sales of batteries count at billions of dollars annually, there is still room for alternative technologies. Since the research and development in electrochemical technology have been conducted for a long time, the technology is quite mature and no major breakthrough is expected in this field in the near future. The alternative energy-storage technologies are super-capacitors, super-conducting magnetic energy systems (SMES), and flywheels. Among them, the flywheel system is the most promising technology for replacing the traditional electrochemical batteries as an energy-storage solution for a variety of applications, including power quality, UPS systems, telecommunications, land vehicles, and aircraft.

The concept of storing energy in flywheels mechanically as kinetic energy is quite old; but recent advancements in new materials science, magnetic bearing control, adjustable speed drives, and power electronics have revived interest in this old concept. Traditionally, flywheels were used only as high-power energy-storage devices for ride-through applications with a duration of several seconds. However, nowadays, there are flywheels on the market that can provide energy in the kWh range [29, 30].

1.3.1 Fundamentals

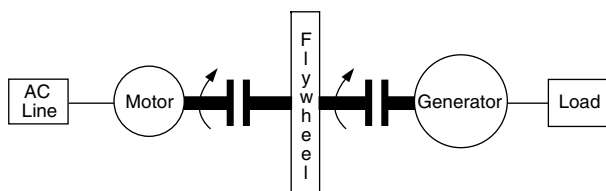
Flywheels are one of the oldest, simplest, and most common mechanical devices. Although when we talk about the flywheel battery, we think about a rotating mechanical device. It actually includes a motor/generator (M/G), a flywheel, a bidirectional converter, and control and communication circuitry. The concept of a typical flywheel battery is shown in [Figure 1.16](#).

**FIGURE 1.16**

The modern concept of flywheel battery application.

The motor spins the flywheel, which stores kinetic energy. When it speeds up, it accumulates energy; when it slows down, it delivers energy. In the past, flywheels were used in a system where a large-mass flywheel was coupled with a rotating motor-generator unit, as shown in Figure 1.17.

Because of the fact that the flywheel and generator rotate at a system-dependent speed and the permissible frequency tolerance of the generator voltage is very narrow, the system could only deliver about 5% of its stored energy [31–33]. Recent advancements in power electronics and adjustable speed drives have allowed the development of highly efficient flywheel storage systems that are not system-dependable. A typical choice of a motor-generator is a permanent magnet, brush-less machine due to its high efficiency, low rotor loss, high-power weight ratio, and low noise [34]. Magnets with high-energy products such as neodymium–iron–boron are usually used. However, permanent magnet materials with high-energy products are prohibitively expensive. Synchronous reluctance and switched reluctance machines can compete with

**FIGURE 1.17**

The old concept of flywheel battery application.

permanent magnet machines in flywheels applications since they can achieve a high efficiency and do not require expensive materials [35].

One of the main components of the flywheel battery is the flywheel rotor, which we will henceforth call flywheel for simplicity. The flywheel is a rotating mass that stores energy mechanically in the form of kinetic energy. Kinetic energy stored in a rotating object is proportional to its moment of inertia and to the square of its rotational speed:

$$\text{Kinetic Energy} = \frac{1}{2} \times I \times \omega^2 \quad (1.5)$$

$$I = k \times M \times R^2 \quad (1.6)$$

where I is the moment of inertia, ω the rotational speed, M the mass, R the radius, and k the inertial constant, which depends on the shape of the object ($k = 1$ for rim and $k = \frac{1}{2}$ for a solid disk of uniform thickness).

From Equation 1.5, it is obvious that for a given rotational speed, the amount of kinetic energy stored is larger for a larger mass. As a result, in the early years of development of flywheel technology, high-density materials, namely metals, were the natural choice for the flywheel rotors.

In order to optimize the energy-to-mass ratio, it is better that the object rotate at the maximum allowable speed. However, the centrifugal force for a rotating object is proportional to the mass of the object and to the square of its rotational speed as follows:

$$F_{\text{centrifugal}} = M \times R \times \omega^2 \quad (1.7)$$

This centrifugal force can rip a rotating object apart. Hence, while dense materials can store more energy, they are also exposed to greater centrifugal force. As a result, they fail at lower rotational speeds than the low-density materials with higher tensile strength.

Recent advancements in the development of different composite materials give the flywheel designers a new choice of material for the flywheel rotor, which allows much higher rotational speed. Different high-strength fiber composites are used depending on whether the designer wants maximum energy storage-per-unit-volume, as in aircraft or vehicular applications, or requires maximum energy storage-per-unit-cost, as in stationary applications. The cost for different composite materials can range between \$12 per pound and \$60 per pound [34] with quite different specific strengths [32].

The use of modern high-strength composite materials allows the design of an ultra-high speed flywheel system. However, the high speed brings new challenges. First, the use of conventional mechanical bearings makes no sense at such high speeds. Instead, advanced magnetic bearings are used. Active magnetic bearings are inherently unstable and require complicated control. In addition, the high level of aerodynamic losses at high speeds requires most high-speed flywheels to spin in a partial vacuum.

Safety requirements require containment of the whole system, which can assure that all the disintegration products at burst failure are kept within the containment.

1.3.2 Classification

Flywheels can be classified into two groups based on the rotor speed: low-speed and high-speed flywheels.

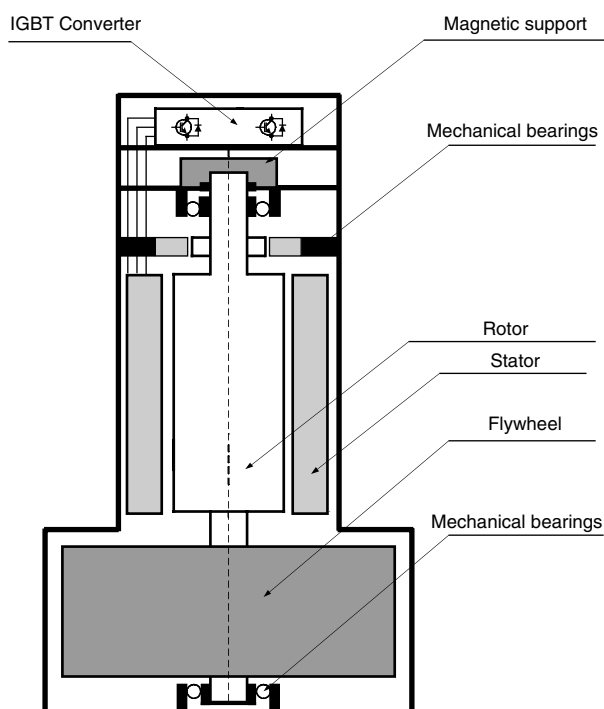
1.3.2.1 Low-Speed Flywheel Systems

Low-speed flywheels rotate at up to 6000 rpm. The flywheel is usually made of high-strength engineering steel. Since the speed is not very high, the aerodynamic drag losses are not considerable; therefore, it is not necessary to operate the flywheel in a vacuum. A partial vacuum or lighter gas can be used to reduce the aerodynamic losses. Since the stored kinetic energy is proportional to the square of the speed and the speed is limited to not very high levels, a considerably larger inertia is necessary for low-speed flywheels, which results in a larger weight. Consequently, magnetic support for the conventional bearings is advisable to increase the bearings' life. Sometimes, even magnetic bearings can be employed. Low-speed flywheels are usually designed for short discharge times and are also referred to as power wheels. The rate at which energy can be recharged into or drawn out of the system is limited only by the motor-generator design; therefore, most of the cost goes toward the motor-generator unit. Since the motor-generator design is quite mature, the cost of the whole system is lower than that of the high-speed flywheels. The output frequency of the generator is between 100 and 200 Hz. For a motor-generator unit, both permanent magnet and conventional excitation can be considered. The principle design of the low-speed flywheel is shown in [Figure 1.18](#).

Compared to the high-speed flywheels, weight and space requirements of the low-speed storage systems are doubled; but, the simpler construction results in lower cost, approximately five times lower. Low-speed systems are used only in stationary applications where cost considerations are of primary concern.

1.3.2.2 High-Speed Flywheel Systems

High-speed flywheels rotate at speeds above 10,000 rpm up to 100,000 rpm. Such high speeds are possible because of the relatively small mass moment of inertia of the rotor. It is wound from high-tech compound materials with a specific strength, five times higher than the steel. The high speed of the rotor allows for a much higher amount of energy to be stored, so the high-speed storage systems can also work as energy wheels. Most of the cost goes toward the energy-storage component. Since the production of the high-tech composite materials is still quite expensive, the overall cost of the high-speed storage systems is high. It is expected that, in the near future, with the advancement of material science, this cost will go down considerably. In addition, conventional bearings at high speed are of no use; therefore, magnetic bearings have to be employed. Furthermore, at such high speeds, aerodynamic losses are considerable. As a result, the rotor has to run in a vacuum. Consequently, no effective cooling can be provided. The rotor cannot have windings and is excited by

**FIGURE 1.18**

The principal design of a low-speed flywheel system.

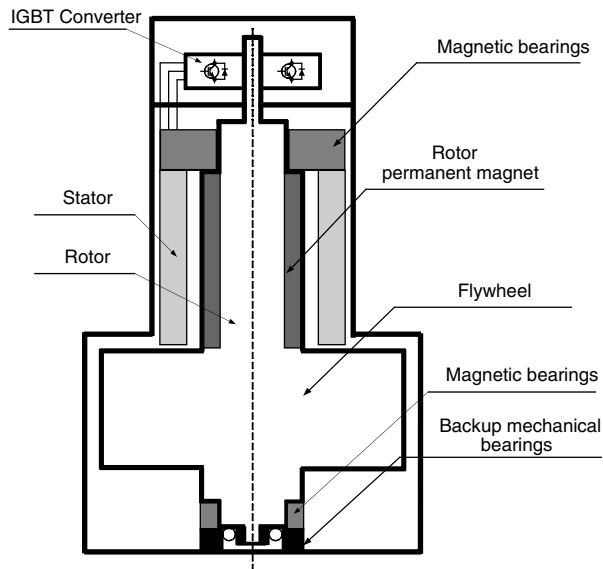
permanent magnets. During the standby mode, hysteresis losses are produced in the stator core. To limit them, an ironless gas ceramic stator is used. A principal design of a high-speed flywheel system is shown in [Figure 1.19](#).

For safety reasons, the whole system is placed in a containment that is capable of containing a loose rotor reaction or any other event, which can occur at the maximum operating speed. The output-generated voltage is unregulated in the range of a few kHz. The bidirectional converter has to be designed for both maximum voltage at high speed and maximum current at low speed. The high-speed flywheels have a low weight, small size, and high energy density, which make them suitable for vehicular applications. However, the technology is relatively new and not widely proven in the field.

1.3.3 UPS Applications of Flywheels

In some UPS applications, flywheels are a better solution than the traditional VRLA batteries. Some of the features of such UPS applications are as follows:

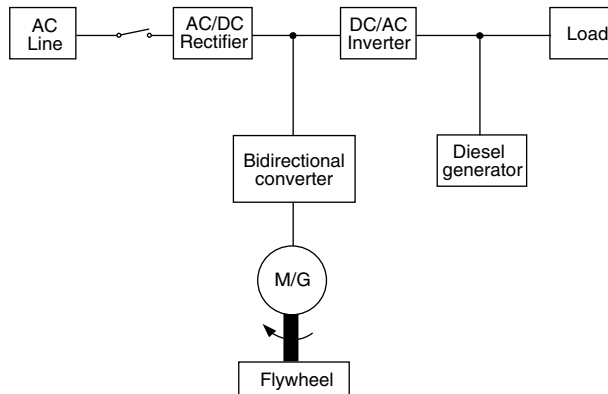
- A power rating of more than 200 kVA.
- Disturbances in the system are often and short, less than 1 min in duration.

**FIGURE 1.19**

The principal design of a high-speed flywheel system.

- The system requires a diesel generator.
- Space is a critical design parameter.
- The customer is willing to consider life cycle cost over the up-front cost.

In such UPS applications, flywheels are much more effective than the VRLA batteries. A basic circuit diagram of such a configuration is shown in Figure 1.20. It consists of a rectifier/charger, a flywheel system, and an inverter [36]. The rectifier/charger continuously supplies the DC bus with power. Its power

**FIGURE 1.20**

A basic circuit diagram of the flywheel-based UPS system with a diesel generator.

rating is required to meet 100% of the power demanded by the load as well as the power demanded for charging and speeding up the flywheel. The flywheel is rated to supply power to the load during the backup time when the AC line is not available. The duration of this time depends on the start-up characteristics of the diesel generator and varies with different generators. The inverter is rated at 100% of the load power since it must supply the load during the normal mode of operation as well as during the backup time.

In other applications, flywheels are used along with the VRLA batteries in a hybrid UPS system [32]. A principal circuit of such a UPS is shown in Figure 1.21.

The flywheel system operates at voltages higher than the battery set. In this way, all short outages (more than 97%) are handled by the flywheel and only long outages are backed up by the battery set. This allows optimal design of both energy-storage systems — the flywheel system for the high-power application and the battery system for the high-energy application. The battery life is highly extended because most of the time the batteries remain in the standby mode and do not go into frequent discharge. Discarding in this way the weakest point of UPS systems, the unreliability of the VRLA battery, the overall system design results in a highly reliable UPS system.

Other applications of flywheel energy storage systems include vehicular, aerospace, distributed generation, and power quality applications.

In hybrid electric vehicles (HEV), some type of energy storage device is necessary to store the excess of energy from the internal combustion engine (ICE) and to drive the vehicle when the energy from the ICE is not enough. This is a typical high-power, high-cycle application. Flywheels have clear advantages over the electrochemical batteries here. If we consider regenerative braking, for example, when the vehicle is slowed down, a huge amount of energy is released for a very short time. Electrochemical batteries have an inherently slower rate of absorbing high power than the flywheels. Some advantages that

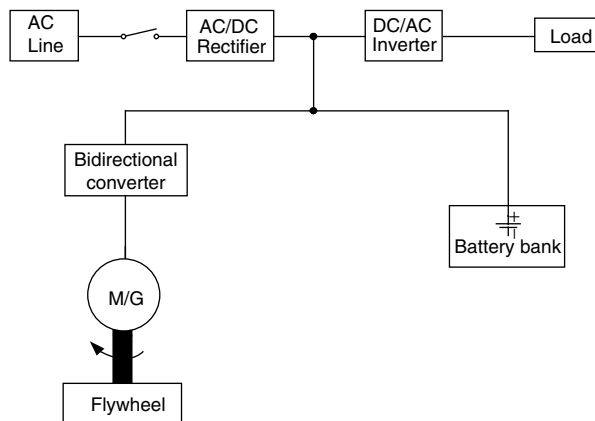


FIGURE 1.21

A basic circuit diagram of the flywheel-based UPS system with a battery bank.

make flywheels more attractive than the electrochemical batteries for vehicular applications include a high-power capability, longer life, compactness, and lower weight. The compactness and lower weight come from the fact that flywheels can be deeply discharged and, as a result, do not need oversizing of the system, as is the case with the electrochemical batteries.

In the international space station (ISS), the energy storage system is a vital issue. The reliability is of the highest concern. In this sense, the superiority of flywheels over the electrochemical batteries is obvious. Monitoring of the state of charge and state of health of batteries is difficult and not highly reliable, while monitoring of flywheels is very reliable. A flywheel energy storage system is under development by the National Aeronautics and Space Administration (NASA). The initial results show that its life is three times longer and it can power the load for twice as long as a chemical battery, while the space and weight for both systems are the same [31].

Most of the distributed generation systems rely on stored-energy systems for proper operation. While electrochemical batteries are a good solution for load leveling, they are expensive and highly inefficient for load following applications. Flywheels with their high-power capabilities are perfect for such applications. In this sense, flywheels can increase the reliability and quality of the distributed generation systems based on fuel cells, photovoltaic arrays, wind turbines, and cogeneration gas turbines.

Nowadays, consumers require not only power with high reliability but also with high quality. About 97% of all power line disturbances last no longer than 3 sec [33] and more than 80% of them last less than 1 sec [31]. Chemical batteries are highly inefficient if a backup time of less than 1 min is required. This is an area of application preserved exclusively for flywheel systems. In fact, this is the most well-known commercial use of flywheels.

1.4 Comparative Analysis of Flywheels and Electrochemical Batteries

Flywheels are unique among the energy-storage devices with their ability to supply very high power. In fact, the rate at which energy can be recharged into or drawn out of the flywheels is limited only by the motor-generator design and can be very high. It is quite a different situation with lead-acid batteries. The rate of discharge in lead-acid batteries is proportional to the surface area of the plates and the internal resistance of the battery. The larger the area, the higher the rate of discharge, and the lower the internal resistance, the higher the current capability of the system. In order to increase the surface area of lead-acid batteries, designers have two options. The first is to make plates thinner and the other is to use more plates. The inherent problem with the first approach is that battery life is proportional to the thickness of plates: the thinner the plates, the shorter the life. The problem with the second approach is that, while the surface areas increase with an increase in

the number of plates, the capacity also increases. Therefore, eventually the designer oversizes the capacity, which results in a higher cost, weight, and volume of high-power VRLA batteries.

Decreasing the internal resistance of the batteries leads to other problems. In order to decrease the internal resistance, battery designers remove the fiberglass mat surrounding the positive plate. Instead, they mix the active materials with the integrated fibers. This reduces the battery impedance, but leads to two problems that reduce the battery life. First, the PbO_2 sedimentation is much higher. Second, the low internal resistance causes problems with DC and AC ripples of the voltage across batteries [26].

Battery designers try to find the optimal compromise between all these issues in order to design batteries with a high rate of discharge. These efforts have led to the development of modern UPS batteries, which are capable of supplying high currents for a short period of time, that is, 10 to 60 min, in contrast with the traditional lead-acid batteries with a rate of discharge of 5 to 20 h. However, there are still many problems regarding the lead-acid batteries for high-power applications, such as

- a slow recharge rate,
- a narrow temperature operation range,
- no reliable method for monitoring the state of charge and state of health, and
- environmental issues.

Flywheel energy-storage systems provide a complete solution for all of the above problems. They have a very fast recharge rate and low temperature sensitivity. They are environmentally friendly. Monitoring is very reliable. By observing the speed, one can always see how much the stored energy is. Flywheels require very low or no maintenance. Furthermore, the rate of conversion of kinetic energy into electrical energy is limited only by the generator design, which makes flywheels extremely well suited for high-power applications. Flywheel energy-storage systems, however, should not be considered as a replacement for the electrochemical lead-acid batteries. Rather, they should be considered as a competitive alternative in high cyclic applications, where issues like duration of life, volume, weight, maintenance, temperature sensitivity, environment, and reliability are critical. Some examples of such applications are vehicular and aerospace applications, power quality applications, distributed generation, and UPS systems.

1.5 Applications of UPS Systems

In the past, UPS systems have been used as large installations in hospitals, telecommunication facilities, and data centers. Their main purpose was to supply the load during blackouts and the only available topology was the so-called on-line UPS. Later, the off-line UPS systems appeared on the

market in response to the demand for small and inexpensive UPS systems designed to supply a particular small load. The main applications are personal computers. Then, line-interactive UPS systems came as a compromise between high-performance, but expensive on-line topology, and the less expensive, but poorer performance off-line topology [14]. At the beginning, their range of applications was in the low- and medium-power range; but now, the new delta-conversion line-interactive UPS systems have applications in installations of a few MW [15, 17, 37–39].

UPS systems not only supply energy during blackouts but also in most cases, provide some kind of power conditioning. This additional function of the UPS systems stems from two facts. First, loads are now much more sensitive to the quality of power than in the past. Second, nowadays, the power quality deteriorates as a result of the fact that utilities try to operate the systems as close to their limits as possible in order to be more competitive on the market. Today, UPS systems have much more diverse applications than in the past. They are now not only highly desirable but also a required standard in many cases.

There are presently two tendencies in UPS system development: distributed and centralized.

1.5.1 Distributed Approach

In a distributed approach, many separate UPS units operate in parallel to supply critical loads. UPS units are placed flexibly in the system to form a critical load network. A typical distributed UPS system is shown in Figure 1.22.

Distributed UPS systems have many advantages. They are highly reliable because of the redundancy. In fact, it is easy and inexpensive to achieve the so-called $N+1$ redundancy in distributed UPS systems, where N UPS units supply the load and one additional unit remains in reserve. The second advantage of the distributed UPS systems is their high flexibility. It is easy to increase the capacity of the system, when the load grows, by simply adding additional units. Another advantage is that the system is user-friendly with regard to

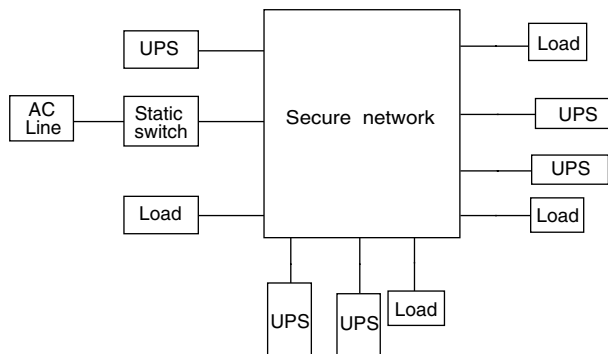


FIGURE 1.22

Block diagram of a typical distributed UPS system.

maintenance because of the $N+1$ redundancy. We can simply turn off the defective unit for maintenance, while the system continues to operate using the remaining units. There are problems associated with distributed UPS systems. First, the load sharing between separate units has to be very fast and precise because of the fast dynamic response of each module and the low overload limit of a typical static UPS. In practice, this load sharing is difficult to achieve and requires very fast and complicated digital controllers. Second, monitoring the whole system is difficult and requires specially trained staff. Instead, the monitoring is separated between many people and as a result the reliability of the system as a whole decreases [23].

The distributed approach is expected to be more attractive for highly proliferated loads such as medical equipment, data processing, and telecommunications.

One interesting application in telecommunications is the combination of UPS systems and fuel cells, which replace the usual diesel generator [40]. Generally, the use of any kind of renewable energy source, such as photovoltaic arrays, wind turbines, or hydroturbines, in combination with UPS systems, seems attractive from an environmental point of view [41].

1.5.2 Centralized Approach

In the centralized approach, one large UPS unit supplies all the critical loads and the main aim is to ensure the continuous operation of the whole process rather than the operation of specific critical loads. This approach is more desirable for industrial and utility applications. The problems here are associated with the high relative cost for achieving redundancy and increasing the capacity with expansion of the load.

The centralized approach offers a clear advantage with respect to the maintenance and service of the UPS systems. A specially trained group of staff will be in charge of maintenance and service, reducing the risk of misuse of the system and increasing its reliability. The use of line-interactive topology in centralized UPS systems can provide some additional useful functions apart from ensuring the continuity of the power supply. By using a parallel-connected UPS to control the real and reactive power drawn from the AC line, one can use it for load leveling, voltage regulation, harmonic suppression, or reactive compensation.

Load leveling function is achieved by controlling the real power drawn from the AC line. It can be done by controlling the phase angle between the AC line voltage and the inverter's output voltage. In this way, the real power drawn from the AC line during the high price time zone of the day can be fixed to a particular level and the rest of the real power demanded by the load is supplied by the UPS. During the low price time zone, only the AC line supplies the load and the UPS draws additional real power to recharge the batteries. Of course, in order to implement this function, the capacity of the batteries must be higher than the usual capacity required for supplying the load during blackouts.

The voltage regulation is easily achieved by controlling the reactive power supplied by the inverter. This control is done by alerting the amplitude modulation index of the inverter and from here the magnitude of the output voltage. This action is independent of the AC line voltage; hence, the voltage regulation is very robust. It is also easy to drive the inverter to compensate the reactive power demanded or produced by the load and, at the same time, to absorb any harmonics caused by the nonlinearity of the load. In this way, a high power factor can be achieved, which helps to better utilize the whole system and additionally to save on the energy bill.

This additional capability of the line-interactive UPS systems to control the real and reactive power flow from the AC line is valuable from the power system operation and control standpoint [42, 43]. Utilities use parallel UPS systems. They call them battery energy-stored systems (BESS) for load leveling, voltage stabilizing, frequency control, and active filtering. As a load-leveling device, BESS helps to cover the peak power demanded by the loads. It is well known how useful, from a power system operation point of view, a unity load power factor is.

BESS can also work as a frequency control device if its capacity is large enough compared to the overall power of the system. It can supply additional real power to the system in the case of generator outage in order to stabilize the frequency. The BESS working as a voltage stabilizer or as an active filter has already been explained.

By rapidly controlling both real and reactive power flow from a BESS, the power system operator is provided with a powerful control device against any oscillations in the system. In many features, a BESS resembles flexible AC transmission systems (FACTS) by controlling the voltage and phase angle out of the three parameters necessary to control the power flow in a power system: voltage magnitude, phase angle, and impedance. Full control over these three parameters can be achieved by the integration of series and parallel converters connected by a common DC-link. This system can be utilized as a power flow controller device for real-time-controlled FACTS [44]. The same approach can be used to improve the power quality at the point of installation on power distribution systems or industrial consumers. The so-called unified power quality conditioner (UPQC) can stabilize the voltage and compensate for reactive power, negative-sequence currents, and harmonics [45]. The same configuration is used to develop the latest line-interactive delta-conversion UPS systems. It overcomes the main drawback of the conventional line-interactive topology, that is, the inability to control, simultaneously, both the output voltage and the input current.

1.6 Parallel Operation

With the present rapid growth of loads especially sensitive to the quality of supplied power, UPS systems are becoming a necessity in many applications

such as medical facilities, life-support systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and on-line management systems.

There are two independent approaches in UPS systems: centralized, in which one large UPS unit supplies all the power demanded by the load; and distributed, in which a multiunit system operated in parallel supplies the power [23]. Both approaches have advantages and disadvantages, which have been discussed in previous sections. The centralized approach is impractical for some applications because of its high initial cost, site installation difficulties (large size and weight), and reduced reliability (single point of failure). The advantage of parallel multiunit UPS systems is especially apparent in high-power applications. Here, because of the limited battery voltage, high battery currents, sometimes up to kA, have to be drawn if a single unit is used. When several units are used, this high current is split between them, substantially reducing the overall price of the system [46]. Another advantage of the parallel multiunit UPS systems is that the reliability of the system can be improved by using the so-called $N+1$ redundancy. Here, N separate units continuously supply the load, and one additional unit remains in reserve. If one of the N operating units fails, it is turned off and the reserved unit starts operating instead. The failed unit can be repaired or replaced while the whole system continues to work.

The parallel UPS systems are also very flexible toward an expansion of the load. The capacity of the UPS can easily improve by simply adding additional modules.

1.6.1 Configurations

A typical on-line UPS consists of an AC/DC rectifier, a battery bank, and a DC/AC inverter. The concept of parallel operation can be applied to rectifiers alone, to inverters alone, or to the whole UPS. As shown in Figure 1.23, two or more AC/DC rectifiers can operate in parallel to supply the DC-link with rectified voltage/current. On the other side of the DC-link, one or more inverters supply the critical loads.

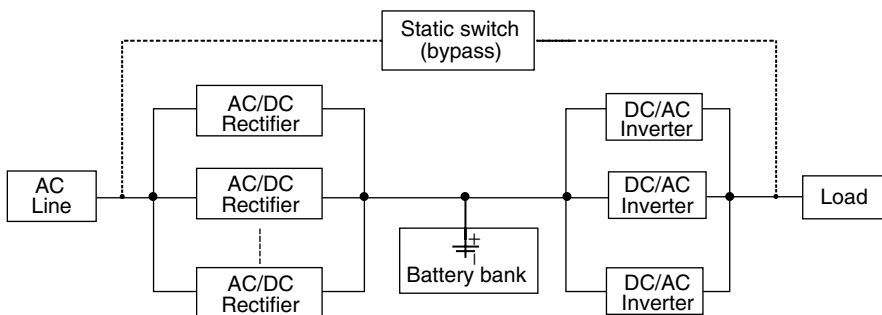
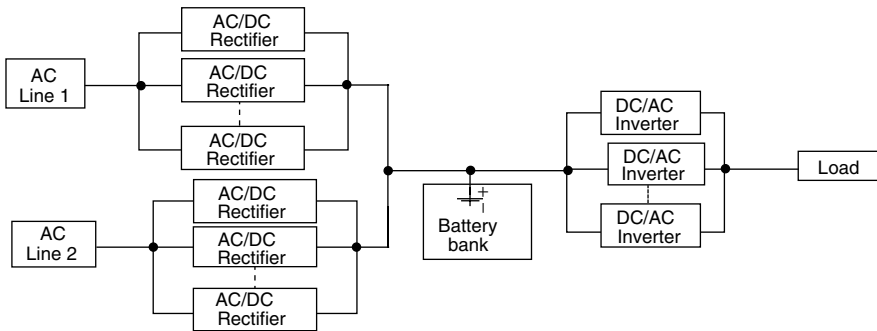


FIGURE 1.23

Block diagram of a typical on-line UPS with several rectifiers in parallel.

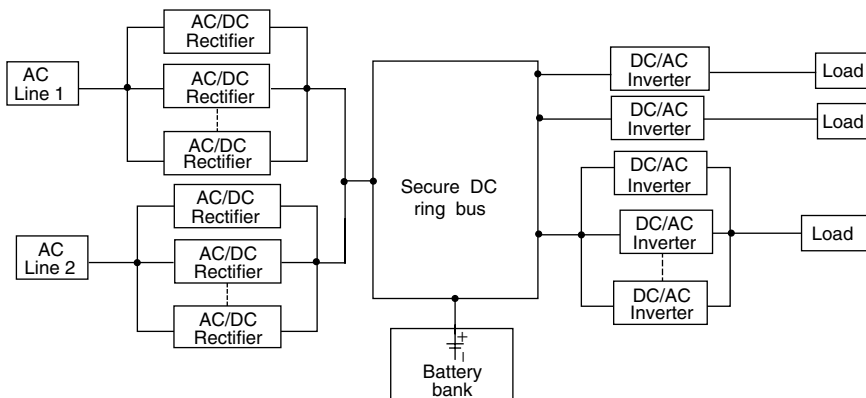
**FIGURE 1.24**

Block diagram of a typical on-line UPS with two dedicated AC lines.

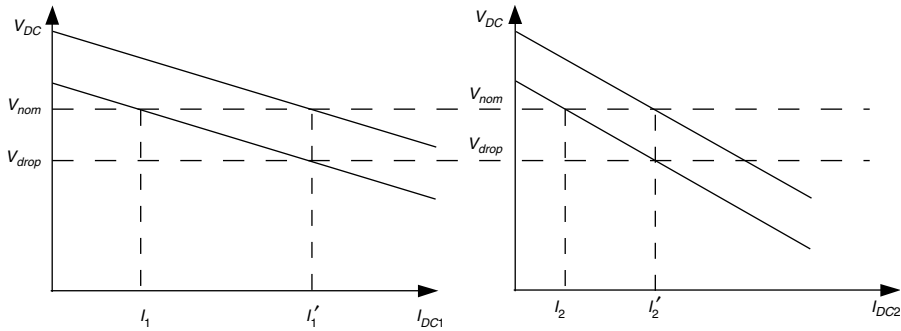
The reliability of the system can be improved if two dedicated AC lines supply two separate rectifiers or two separate groups of rectifiers, as shown in Figure 1.24. The dedicated lines help to isolate the DC-link from the effect of the other loads on the AC line side. Each of the two rectifiers or each of the two separate groups of rectifiers is capable of supplying the full rated system load. This ensures redundancy of the power sources.

The concept of parallel operation can be taken further, as shown in Figure 1.25, where two separate rectifiers fed from separate AC lines formed a DC ring bus [47]. The rectifiers can be placed far from each other and do not require communication with each other. The load sharing is achieved by a built-in voltage drop. In fact, changes in DC voltage are used as the communication signals.

The principle of operation of the UPS systems in Figure 1.25 can be explained with the aid of Figure 1.26. A change in load causes a corresponding change in DC voltage. For example, a load increase causes a decrease in DC voltage. Rectifiers work in voltage control mode to increase their currents in

**FIGURE 1.25**

Block diagram of a typical UPS with several rectifiers in parallel forming a DC ring bus.

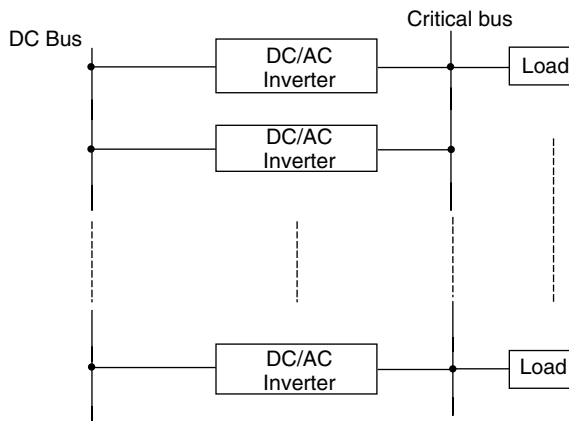
**FIGURE 1.26**

Voltage drop characteristics of the rectifier groups in [Figure 1.25](#).

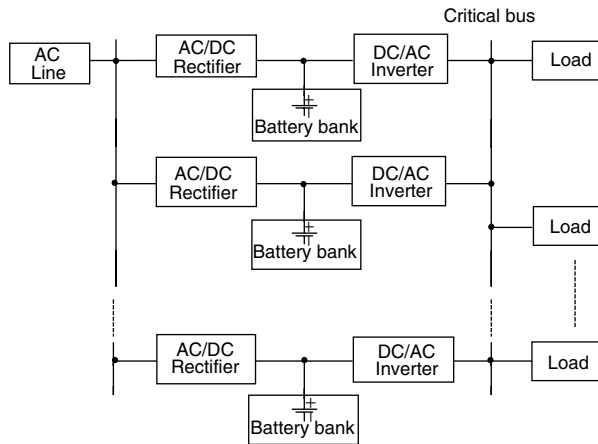
order to restore the proper voltage level. The overall increase in current ($\Delta I = \Delta I_1 - \Delta I_2$) is distributed between the separate rectifiers by the built-in voltage drops that the steeper the voltage drop, the less the load taken from the rectifier as shown in [Figure 1.26](#). The configuration shown in [Figure 1.25](#) is used mostly in industrial applications, where many different critical loads have to be supplied.

One additional advantage of such a system is that critical loads can be categorized by importance. The lower-priority loads may be switched off at a higher DC-link voltage. Therefore, the duration of the backup time for the most important loads can be extended.

The concept of parallel operation can also be applied to inverters [46]. Two or more inverters fed from a common DC-link supply loads connected to a critical bus, as shown in [Figure 1.27](#).

**FIGURE 1.27**

Block diagram of a typical UPS system with several inverters in parallel.

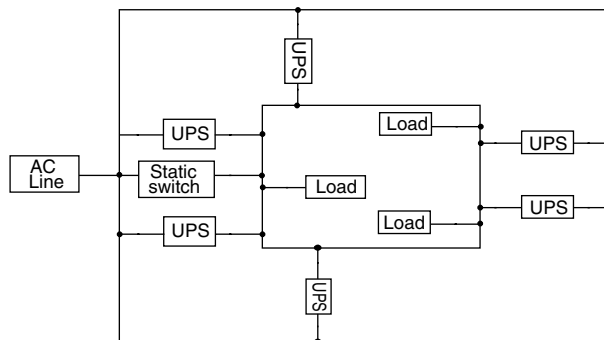
**FIGURE 1.28**

Block diagram of several on-line UPS systems working in parallel.

In Figure 1.28, several UPS units operate in parallel [48–51]. The modules are close to each other and parallel operation is achieved by communication between separate units.

A real distributed UPS system requires UPS units to be placed flexibly in the system building or industrial plant, forming the so-called secure network from which different critical loads are supplied [14, 48]. Such a distributed UPS system is shown in Figure 1.29.

Because a real distributed UPS system requires separate UPS units to be placed arbitrarily in the system, often far from each other, communication between them is impractical. Hence, the communication between separate units need not be decisive for proper parallel operation of the units. It can only enhance the performance of the system. The parallel operation of the separate units has to rely only on locally available parameters — voltage, current, and frequency. Similar to the control of the two rectifiers in Figure 1.25, inverters

**FIGURE 1.29**

Block diagram of a distributed UPS system.

in Figure 1.26 use the phase angle between the output voltages to control the real power flow and the magnitude of the output voltages to control the reactive power flow [14, 48, 51]. This is done by introducing built-in frequency and voltage drop characteristics in each inverter. The regulation of real and reactive power flow between separate units is explained in detail later in the discussions of the wireless independent control.

1.6.2 Fundamental Principles of Parallel Operation

The stable operation of a power system needs an exact balance between the generated and consumed real and reactive power. In this sense, implementing a good control over both P and Q is essential from operational and control points of view. The real power and the reactive power transferred between an inverter with output voltage V_{in} and a critical bus with voltage V_c are described by

$$P = (V_{in} V_c \sin \delta) / Z \quad (1.8)$$

$$Q = (V_{in}^2 / Z) - (V_{in} V_c \cos \delta) / Z \quad (1.9)$$

When V_{in} and V_c have the same phase, but different amplitudes, there is reactive power circulating. When V_{in} and V_c have the same amplitude, but different phases, there is active power circulating. When V_{in} and V_c differ in both phase and amplitude, there is active and reactive power circulating. When the power angle δ is small, which is usually the case, the real power flow depends primarily on δ , and the reactive power flow depends primarily on the voltage magnitude V_{in} . Control of frequency dynamically controls the power angle and, as a result, the real power flow. Because of the very low output impedance Z of the typical UPS inverter, even a very small value of δ results in a very large imbalance in the active power flow. Typically, a one-degree difference in phase leads to about 50% power disturbance. Under light loads, some inverters may be operating as rectifiers. Therefore, the output voltage of all inverters working in parallel must be kept strictly in phase by a PLL in order to guarantee equality of the output active power for the corresponding inverters. Even after all output voltages are locked in phase, reactive currents can still circulate between some inverters if their output voltage magnitudes differ from each other. This overloads the inverters unnecessarily. Since the overload capability of a typical static UPS is relatively low, usually 150 to 200%, it is obvious that good control over the output voltage magnitude of each inverter in parallel is essential. Basically, the control over frequency and voltage magnitude should not be too difficult to implement. The problem stems from the fact that UPS designers try to build UPS systems with very fast dynamic response characteristics in order to achieve good performance under nonlinear and step-changing loads. As a result, inverter output currents change quite rapidly. This, combined with the limited overload capability of the UPS, causes difficulties in the control of parallel operating inverters in UPS systems.

1.6.3 Control Strategies in UPS Parallel Operation

1.6.3.1 Concentrated Control

In this control method, as shown in Figure 1.30, a PLL in each inverter is used to synchronize its output voltage in frequency and phase with the voltage of the critical bus, ensuring proper real power load sharing between separate inverters. A parallel control unit detects the total load current I , divides it by the number of inverters n in the system, and passes the signal I/n to each inverter. This signal is used as a reference for the minor current control loop, which takes the current through the output filter inductor as a feedback signal. Both signals are compared and an error is obtained, which is used to compensate any inequality in the voltage amplitude of different inverters. Therefore, a proper reactive power load sharing is achieved [51].

1.6.3.2 Master–Slave Control

Basically, the master–slave control is the same as the concentrated control. The difference is that only the master unit has enabled the PLL, which is in charge of providing a constant sinusoidal output voltage synchronized in frequency and phase with the critical bus voltage. The other inverters work as slaves, which are controlled to track the reference current provided by the

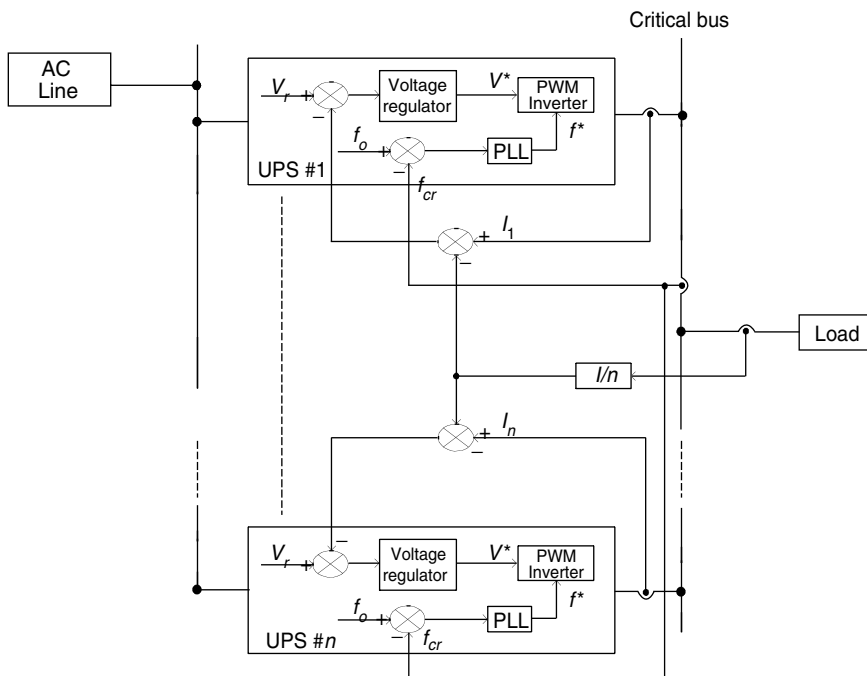


FIGURE 1.30

Block diagram of a typical concentrated control strategy.

parallel control unit. The parallel control unit has the same function as in a concentrated control method. Hence, the reference current derives from the load current; therefore, it can serve as a frequency and phase reference as well. As a result, the slave units do not need to have separate PLL circuits enabled. If the master unit fails, one of the slave units replaces it by simply enabling its PLL circuit [46, 49–51].

1.6.3.3 Distributed Control

In the two methods described above, a failure in parallel control circuit can lead to the failure of the whole system. This is prevented in the distributed control method. Each inverter sends signals to the others. Compensating voltage and frequency signals are sent to each inverter [51].

1.6.3.4 Wireless Independent Control

In this method, there is no inner-connective load sharing wires between inverters. Control is based on information available locally at the inverter terminals: voltage, current, and frequency. Each inverter has a buildup frequency drop characteristic for real power load sharing and a buildup voltage drop characteristic for reactive power load sharing [14, 48, 51]. It is well known that when there is an imbalance in the generated and consumed real power in the system, there is a change in the system frequency. Hence, the frequency can be used as a communication signal between two inverters connected in parallel. For example, if the real power demanded by the two inverters in parallel is increased by $\Delta P = \Delta P_1 + \Delta P_2$, the frequency will initially decline by Δf , as shown in Figure 1.31.

The increase of power ΔP will be taken by the separate inverters according to the slope of their buildup frequency drop. New steady-state equilibrium point will be achieved at a lower frequency. In order to restore the initial frequency, the whole drop characteristic has to be shifted up vertically. A proper active power load sharing control is then implemented without communication needs between inverters. The same strategy is used for reactive power load sharing control; but a voltage drop is used as a communication signal. This control method increases the reliability and flexibility of the

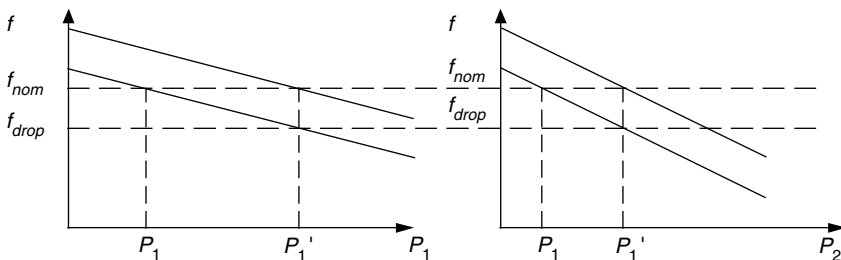


FIGURE 1.31

Frequency and voltage drop characteristics for inverters in parallel.

whole system. It also eliminates any noise disturbances existing in the previously-discussed methods. The essential requirements are high-precision sensors and an extremely high speed in calculation.

1.7 Performance Evaluation of UPS Systems

The performance of a UPS system is evaluated in terms of several factors. The first and the most important factor is the quality of the output voltage. The output voltage should be sinusoidal with a low THD, usually less than 5%, even when feeding nonlinear or imbalanced loads. In addition, UPS systems should have a good transient response toward sudden changes in the load. They should also be capable of maintaining a good output voltage regulation. The circuit configuration and control strategy used are the most significant factors affecting the above mentioned performance features of a UPS.

With respect to the UPS topology, the on-line UPS configuration gives a superior performance followed by line-interactive UPS systems and finally by off-line UPS systems [14]. In on-line UPS systems, the inverter is connected in series with the load in both normal and stored-energy operating modes, and continuously provides power conditioning to the load.

In line-interactive UPS systems, the inverter is connected in parallel with the load and, during the normal mode of operation, provides only limited power conditioning to the load. Only during the stored-energy mode of operation can the performance of a line-interactive UPS be the same as that of the on-line UPS.

The inverter in off-line UPS systems is off during the normal operating mode. Hence, this topology does not provide any power conditioning via its inverter during this mode. Only if it has additional power conditioning circuits can it provide some power conditioning during the normal mode of operation. During the stored-energy operating mode, the performance of an off-line UPS can be the same as an on-line or a line-interactive UPS.

The second important factor in terms of how the performance of UPS systems is evaluated is the power factor of the input current. It is highly desirable if the power factor is unity or close to unity in order to meet the corresponding standards and to utilize the whole system better. The high-power factor means high displacement factor (DF) and low THD of the input current.

There are two techniques for improving the performance of UPS systems: passive and active. The passive technique uses filters for the harmonics in order to prevent them from flowing into the AC line. This is a good technique for low-power cost-sensitive applications.

For higher-power applications, active PFC techniques are used. In these techniques, either a PWM rectifier is utilized [52, 53] or an additional DC/DC PFC circuit is used [54, 55]. Basically, this is a DC/DC circuit that is controlled in such a way that it forces the rectifier to draw a sinusoidal current from the AC line, which is in phase with the input voltage. These active techniques are applicable only for on-line and off-line UPS topologies. For the line-interactive

UPS systems, the PFC is achieved by controlling the power angle between the input and output voltages [15]. It is worth noting that when the inverter has to compensate for a disturbance in the input voltage, such as under- or over-voltage, the PFC function of the inverter has to be sacrificed.

The third important factor for evaluating the performance of UPS systems is the transfer time. In terms of this aspect, the on-line UPS topology is superior. Its configuration naturally ensures that the load is continuously supplied with power without any transfer time [14].

The transfer time in line-interactive UPS systems depends on the time necessary for converting the power flow from the battery bank through the inverter to the load. Improved performance in this sense is achieved by choosing the DC bus capacitor voltage at the battery side to be slightly higher than the floating voltage of the batteries. In this way, when the AC line fails, it is not necessary to sense the failure because the DC bus voltage will immediately decline under the floating voltage of the batteries and the power flow will naturally turn to the load.

Transfer time is the longest for off-line UPS systems, which depends upon the speed of sensing the failure of the AC line and starting the inverter.

The next performance factor of UPS systems is efficiency. In this sense, the UPS systems can be separated into a single conversion topology consisting of off-line UPS systems and line-interactive UPS systems; and double-conversion topology consisting of on-line UPS systems. Single-conversion topology has better efficiency, which should be taken into consideration in some special applications [17, 15].

The last, but not the least important performance feature of UPS systems is reliability. A simple power circuit implies better reliability. Furthermore, the simpler the control technique used, the higher the reliability of the system. The use of a bypass essentially improves the reliability of the UPS systems. This, of course, leads to the requirement of synchronization of the input and the output voltage in order to achieve seamless transition to the bypass mode of operation. As a result, the control circuit may be more complicated.

Another method for improving the reliability of the UPS systems is the employment of the so-called $N+1$ redundancy [23]. Here, N separate modules supply the load with power working in parallel, and one additional module stays in reserve. If any one of the operating N modules fails, it can be switched off and repaired or replaced while the additional module takes its place. The next step in achieving a high reliability is the so-called distributed UPS systems where several UPS systems are placed arbitrarily, making a secure bus from which several different loads are supplied.

1.8 Power Factor Correction in UPS Systems

UPS systems are ubiquitous solutions for power conditioning of critical loads. However, because of the inherent low-input power factor of the

front-end rectifier, the UPS itself is considered as a harmonic pollution source for the utility and near loads. A typical uncontrolled rectifier draws a highly distorted nonsinusoidal current from the AC line. Its distortion factor shown in Equation 1.10 is low and, therefore, its power factor shown in Equation 1.11 is low even when feeding purely resistive loads with a displacement factor $\cos \varphi = 1$. Usually, the power factor is less than 0.65.

$$DF = I_{1, rms}/I_{rms} \quad (1.10)$$

$$PF = P/S = P/(V_{rms} * I_{rms}) = (I_{1, rms}/I_{rms}) \cos \varphi = DF \cos \varphi \quad (1.11)$$

The benefits from a high power factor are well known: better utilization of the whole system and a low EMI. As a result, the International Standard Committee imposed the IEC-1000-3-2 standard, which requires the UPS systems to meet the limits of the input current harmonics. Accordingly, many passive and active power factor correction solutions have been proposed and widely discussed [54, 55]. Generally, the PFC techniques can be classified as passive or active.

1.8.1 Passive PFC Techniques

In passive PFC techniques, passive LC filters are connected at the input of a rectifier. The filter prevents injection of harmonics from the rectifier to the AC line. Passive filters have high efficiency and low cost. Passive techniques are simple and robust; hence, they are very reliable. Yet, the inductor and capacitor are bulky and heavy, which limits their applications as a single solution only in low-power ratings. These techniques are usually used along with different active PFC techniques, which reduce the harmonic and reactive content of the input current, allowing the input filter to be smaller.

1.8.2 Active PFC Techniques

Active PFC techniques can be classified into two types. The first one consists of PWM rectifiers controlled in continuous conduction mode (CCM) to achieve good output voltage regulation and high input power factor. The second one consists of a PFC circuit, which operates in discontinuous conduction mode (DCM) to force the rectifiers to draw sinusoidal currents from the utility. PWM rectifiers controlled in PFC techniques are usually used in high-power applications, especially when high performance is required. The rectifier is controlled by an outer voltage loop for output regulation and inner current control loops for shaping the input current according to their sinusoidal reference. The main problem here is that when driving the rectifier to obtain a high input power factor, substantial low-frequency voltage ripples appear on the DC side. It is essential in UPS applications that these low-frequency DC ripples are reduced as low as possible because the battery impedance is very low and all DC ripple currents generated by the DC voltage ripples flow into the battery.

This results in heating of the battery, which is very detrimental to the battery's state of health as described in previous sections.

It is usually necessary to connect a very large electrolytic capacitor or a passive LC filter to the DC side in order to reduce the low-frequency voltage ripples, as shown in Figure 1.32. However, such a large capacitor or LC output filter is not desirable because of the short lifetime of the capacitor, the inherent parameter variation of the circuit with time, and the impracticality of downsizing the whole system.

Another way of reducing the DC output voltage ripples is to increase the switching frequency. In Nishida et al. [52], a single-phase PWM bridge rectifier, which takes into account the DC-side voltage ripples, is controlled by a predictive instantaneous current control scheme in order to achieve unity power factor. It can be seen that when the switching frequency is increased from 7.2 to 18 kHz, the power factor becomes substantially higher and the DC output voltage ripples become smaller. Increasing switching frequency implies higher losses. Soft-switching techniques, as described in Mao et al. [55], can significantly increase the efficiency of the rectifier.

An essential requirement for all CCM PFC-controlled PWM rectifiers is a precise detection and processing of the input AC line current and precise processing

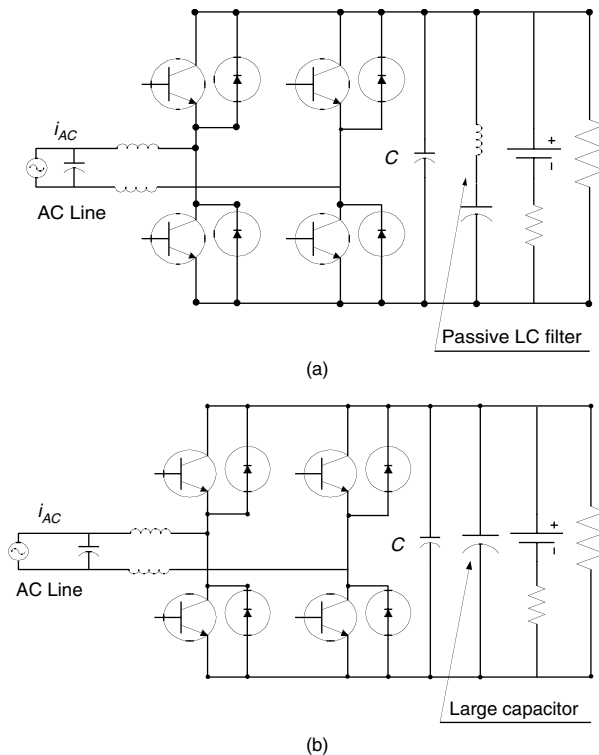


FIGURE 1.32

PWM rectifier with (a) an LC output filter and (b) a large output capacitor.

of the feedback signals, which makes the control circuit more complicated and eventually more expensive. In DCM-controlled PFC circuits, the control strategy is simpler and less expensive. There are two separate approaches in DCM-controlled PFC circuits: double- and single-stage conversion.

In the double-stage conversion PFC approach, as shown in Figure 1.33, the rectifier is followed by an input current shaper stage, which provides power factor correction by forcing the rectifier to draw sinusoidal current, which is in phase with the input AC voltage and with low THD.

It has a loosely regulated output voltage at the intermediate DC bus, which serves as an input to the second stage of a DC/DC converter, which is in charge of providing tightly regulated output voltage to the inverter and to the battery. The efficiency of this approach is not good because of the two power conversion stages. It also requires at least two power switches; but the control is simple and hence the whole system is very reliable. The switch in the input current shaper (ICS) stage is controlled in DCM at a constant frequency. In this method, the peak input current naturally follows the input AC voltage.

A single-stage PFC, as shown in Figure 1.34, integrates the input current shaper and the following DC/DC converter into one single stage. It has one shared switch and one controller. The energy-stored element, usually a capacitor, is placed in series with the load. The single-stage PFC approach usually has a better efficiency; but the control complexity is increased. In addition, the power semiconductor devices may have a higher voltage and current stress than with the two-stage PFC approach. As a result, the single-stage approach is not always better than the two-stage approach in terms of cost and reliability [56]. A combined approach is proposed as a compromise, where a portion of the energy is supplied directly to the load and the rest of the energy is double-converted.

The above mentioned discussions are related to the on-line and off-line UPS systems. For line-interactive UPS systems, the PFC technique is different. Here, the inverter is connected in parallel with the load. It is capable of supplying all reactive and harmonics currents required to keep the power factor close to unity [15, 17–20].

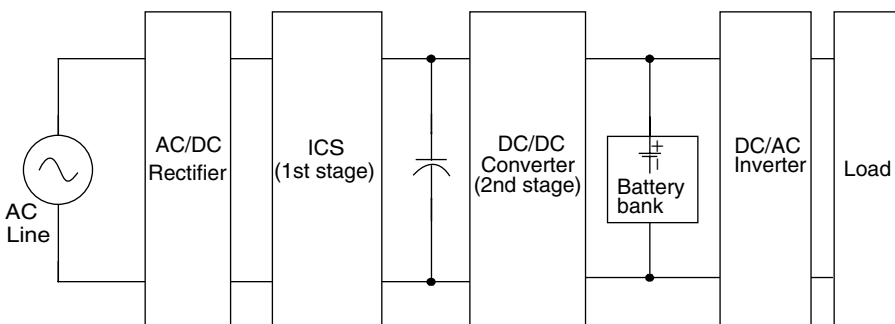
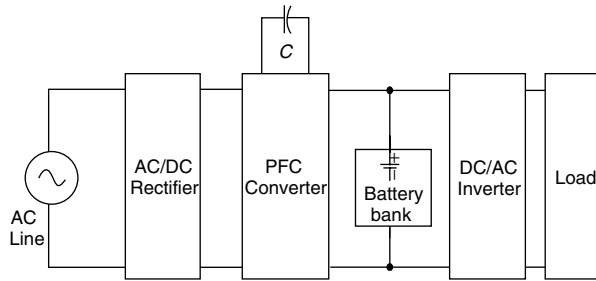


FIGURE 1.33

UPS system with a double-stage conversion PFC circuit.

**FIGURE 1.34**

UPS system with a single-stage conversion PFC circuit.

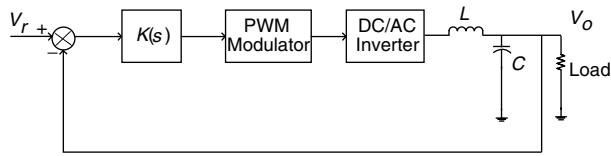
1.9 Control of UPS Systems

THD of the output voltage and dynamic responses of a UPS system are among the most important performance features of the UPS. They depend mostly on the control strategy applied to the UPS inverter. In this sense, the inverter's control strategy immediately follows the UPS topology as the second most important factor, which determines the overall performance of the UPS. The simplest method to deal with a high output voltage THD is to increase the switching frequency and to use appropriate LC output filters. For a given THD, by increasing the switching frequency, the LC filter will be smaller. However, with increasing switching frequency, losses increase accordingly, which is why for high-power rating applications, the switching frequency is limited usually up to 2 kHz.

The aim in the design of the inverter LC output filter system is to achieve zero output impedance, hence zero THD even with nonlinear loads [57]. The problem is that the output filter inductance has some nonzero impedance, which causes distortion in the output voltage when feeding nonlinear loads. Different PWM techniques have been proposed to compensate for filter output impedance and reduce the output voltage distortion. The simplest one compensates only the harmonics caused by the nonlinearities of the inverter, such as blanking time, switching delays, component voltage drops, DC-link voltage fluctuations, and rise and fall times of the devices. However, a sinusoidal voltage at the output of the inverter does not guarantee a sinusoidal voltage at the load terminals. This technique still has a good steady-state performance with linear loads. It is implemented as a single-voltage loop strategy.

1.9.1 Single-Voltage Control Loop Strategy

This strategy, as shown in Figure 1.35, uses a single feedback loop to provide a well-regulated output voltage with low THD. The feedback control can be continuous [58] or discontinuous [59–61]. Analog techniques are used in

**FIGURE 1.35**

Block diagram of a single feedback loop.

the continuous approach. The most usual continuous feedback control is SPWM, which can be of natural sampling type, average type [62], or instantaneous type [63].

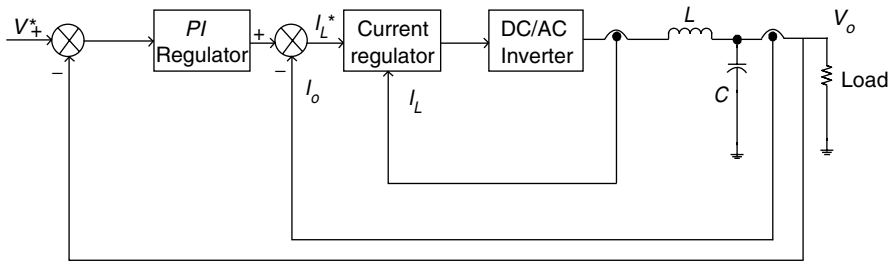
In the natural sampling type, the peak value of the output voltage is detected and compared with a reference voltage in order to obtain the error, which is used to control the reference to the modulator.

The average approach is basically the same; but the sensed voltage is converted to an average value and is then compared with a reference signal. These approaches control only the amplitude of the output voltage and are good only at high frequencies. They are easy to implement; but they have very slow dynamic responses with step-changing and nonlinear loads.

In instantiations voltage feedback SPWM control, the output voltage is continuously compared with the reference signal-improving dynamic performances of the UPS inverter [63]. The speed of the dynamic responses depends only on the switching frequency, which cannot be made very high in higher power rating applications. Another disadvantage of this approach is that harmonics are generated in the output voltage around the switching frequency. In addition, the dynamic response is still not fast enough. Another approach is based on digital control techniques. Discrete-time control strategies are generally of two types: optimum PWM techniques [64] and deadbeat techniques [58–61]. In digital optimum PWM techniques, the switching angles are calculated in order to minimize specific harmonics in the output. These techniques have a very good steady-state performance with linear loads; but with nonlinear and step-changing loads, their performance is unsatisfactory [65]. The deadbeat control technique shows better performance with nonlinear loads. In this technique, based on predicted and sensed output voltage, the exact length of the switching interval can be computed in real time so that the exact value of the desired output voltage can be obtained. The disadvantages of the deadbeat control technique are that it is computationally intensive and, for this reason, it is feasible only at relatively low frequencies. It also shows poor performance with step-changing loads.

1.9.2 Multiple Control Loops

Better performance even with nonlinear and step-changing loads can be achieved by multiple control loop strategies [65]. As shown in [Figure 1.36](#), there are two control loops: an outer and an inner loop. The outer control

**FIGURE 1.36**

Block diagram of a typical control system with multiple feedback loops.

loop uses the output voltage as a feedback signal, which is compared with a reference signal. The error is compensated by a *PI* integrator to achieve a stable output voltage under steady-state operation. This error is also used as a reference signal for the inner current regulator loop, which uses the inductor [65] or the capacitor [66] output filter current as a feedback signal. The minor current loop ensures fast dynamic responses, enabling very good performances with nonlinear or step-changing loads.

The basic current regulators used as minor current loops are hysteresis regulators, sinusoidal PWM regulators, and predictive regulators.

1.9.2.1 Hysteresis Current Control

In a typical hysteresis regulator, the reference signal is compared with the feedback signal. The sign and predetermined amplitude of the error determine the output of the modulator, which has two possible levels $\pm V_{out}$. The duration between the two successive levels of V_{out} is determined by the slope of the reference signal. The output voltage tracks the reference signal within the upper and lower boundary levels $\pm \Delta V$ [67–69]. This hysteresis control has fast transient responses; but the switching frequency varies widely, which is undesirable because it generates additional harmonics. To eliminate this drawback, an improved constant-frequency hysteresis current control regulator can be implemented, as presented in Sae-Sue et al. [68]. In Sae-Sue et al. [68], in order to keep the switching frequency constant, the hysteresis band varies with a function of $\cos(2\omega)$; but the implementation of this technique is complicated.

Hysteresis current controllers have fast transient responses. They are preferred for operation at high switching frequencies. The switching losses restrict their applications to lower power levels.

1.9.2.2 SPWM Current Control

In the SPWM control technique, the output voltage feedback is compared with a sine reference signal and the error voltage is compensated by a *PI* regulator to produce the current reference. The current through the inductor or the capacitor is sensed and compared with the reference signal. After being

compensated by a P regulator, the error signal is compared with a triangular waveform to generate an SPWM signal for switching control. The SPWM current control has a constant switching frequency and also provides fast dynamic responses [66, 67].

1.9.2.3 Predictive Current Control

In this method, the switching instants are determined by suitable error boundaries. When the current vector touches the boundary line, the next switching state vector is determined by prediction and optimization in order to minimize the error [70]. Predictive current control requires a good knowledge of the load parameters.

All these current regulators are typically used as an inner loop to regulate the current in the filter inductor. The current reference for the current regulator is obtained by summing together the error in an outer voltage loop with the actual load current to yield the rated output voltage.

Control for three-phase UPS systems is basically the same. Additional problems are that one must take care of the coupling interference between different phases and unbalanced loads. Generally, for UPS systems operating with fixed-frequency three-phase outputs, control is implemented in stationary (a, b, c) coordinates with correction for phase-lag produced by the control loop [69]. When UPS systems supply a variable frequency application such as AC-adjustable speed drives, the phase error changes with frequency and is difficult to compensate. For such applications, a rotating (d, q) reference frame is preferred, resulting in DC control loops.

1.10 Converters for UPS Systems

A block diagram of a typical single-phase on-line UPS system is shown again in Figure 1.37. It consists of a rectifier, an inverter, a bidirectional DC/DC converter, and a battery bank. In the following sections, a comprehensive review of different converter topologies employed in on-line UPS systems is presented.

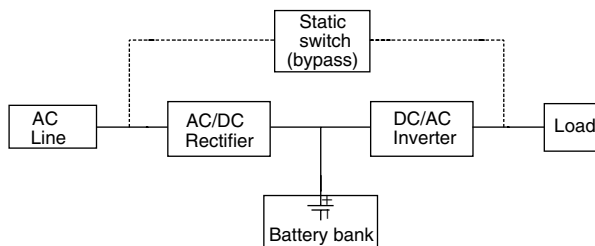


FIGURE 1.37

A block diagram of a typical single-phase on-line UPS.

1.10.1 Rectifiers

The purpose of an AC/DC rectifier in a UPS system is to produce DC voltage with quality sufficient for proper operation of the DC/AC inverter at the back end of the UPS system. Rectifiers are classified into two main categories, uncontrolled and controlled rectifiers, depending on the type of silicon switches used.

1.10.1.1 Uncontrolled Rectifiers

Uncontrolled rectifiers use diodes as switches. A full-bridge uncontrolled rectifier is shown in Figure 1.38.

Diodes D_1 and D_2 conduct during the positive half cycle of input voltage V_s . Diodes D_3 and D_4 conduct during the negative half cycle. Capacitor C is chosen large enough to limit the ripples of the DC voltage to a preset value. Since capacitor C is quite large, the current drawn from the source is highly distorted, as shown in Figure 1.39.

This results in a poor power factor, which is the main drawback of uncontrolled rectifiers. Another drawback of uncontrolled rectifiers is that V_{dc} is equal to the peak input AC voltage. When a higher DC voltage is desired, a voltage doubler uncontrolled rectifier can be employed. Its topology is shown in Figure 1.40.

In this topology, D_1 charges capacitor C_1 to the maximum value of the input voltage during the positive half cycle of V_s . Accordingly, D_2 charges C_2 to the maximum value of the input voltage during the negative half cycle of V_s . The output DC voltage is twice the maximum value of the input AC voltage. Besides the advantage of a higher output DC voltage, this topology also has less number of diodes compared to the full-bridge rectifier. It should be mentioned that the voltage stresses across the diodes for voltage-doubler topology are twice as large as those for the full-bridge rectifier. Another disadvantage of the voltage-doubler topology is that it uses two electrolytic DC capacitors, which are bulky.

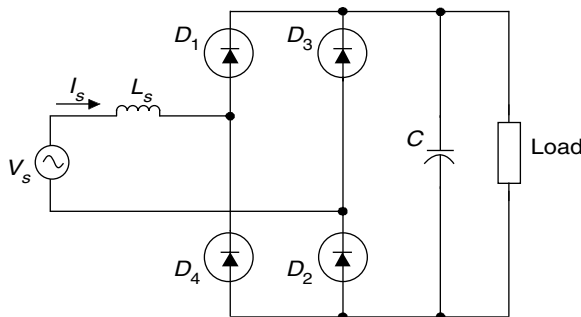
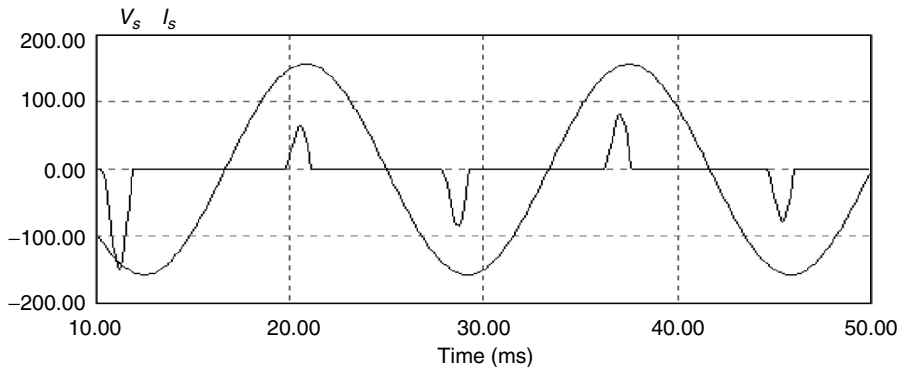
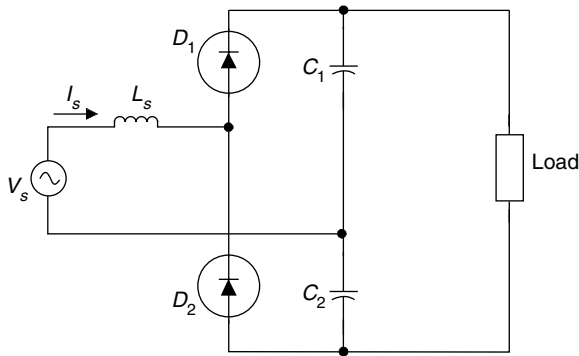


FIGURE 1.38

A full-bridge uncontrolled rectifier.

**FIGURE 1.39**

Input source current and voltage for the uncontrolled rectifier of Figure 1.38.

**FIGURE 1.40**

A voltage doubler uncontrolled rectifier.

The clear advantages of uncontrolled rectifiers are their simplicity, reliability, and low cost. Their main drawback is the poor power factor, which limits the use of uncontrolled rectifiers and opens the market for controlled AC/DC rectifiers.

1.10.1.2 Controlled Rectifiers

Controlled rectifiers use thyristors, MOSFETs, or IGBTs as the switching devices. A full-bridge controlled rectifier with four active switches (IGBTs) is shown in Figure 1.41.

The rectifier consists of switches S_1 , S_2 , S_3 , and S_4 , electrolytic DC capacitor C , and input current shaping inductor L_s . The topology has four different switching vectors: S_1/S_2 , S_1/S_3 , S_2/S_4 , and S_3/S_4 . By switching S_1 , S_2 , S_3 , and S_4 , the input current can be shaped to be sinusoidal and in phase with the input voltage, as shown in Figure 1.42.

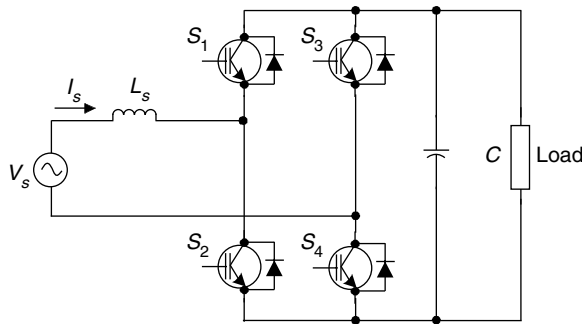


FIGURE 1.41
A full-bridge controlled rectifier.

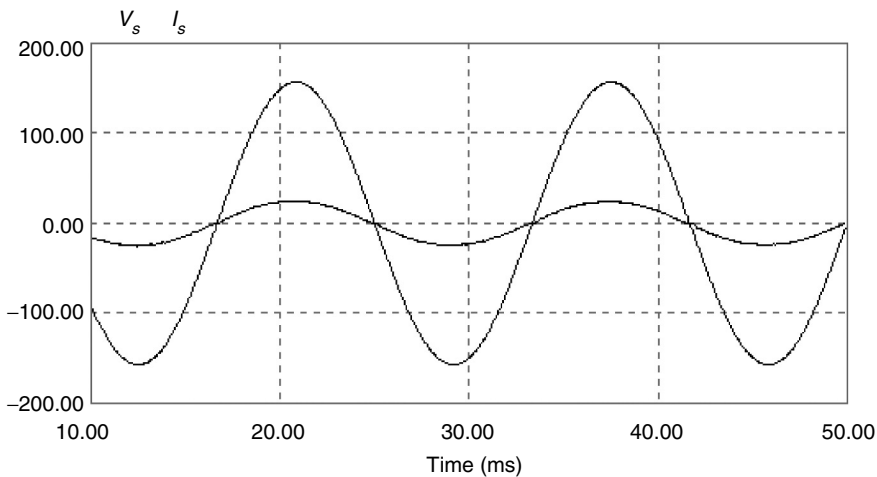


FIGURE 1.42
Input source current and voltage for the controlled rectifier of Figure 1.41.

At the same time, the output DC voltage can be tightly regulated at a preset value V_{dc} , which is always larger than the peak value of the input AC voltage. The simulation result for the DC output voltage is shown in [Figure 1.43](#).

In this way, the tolerance of the on-line UPS system to variations in the input voltage is increased. As a result, the backup batteries do not go into frequent charge/discharge cycling when the input voltage drops a little below its nominal value. This increases the battery life considerably.

The desire to drive the cost down results in different topologies of full-bridge controlled rectifiers with reduced number of switches. In [Figure 1.44](#), a controlled rectifier with two active switches and two diodes is shown.

Switch S_1 shapes the input current during the positive half cycle and switch S_2 shapes it during the negative half cycle. The overall cost of this topology is lower than that of Figure 1.41, with four controlled switches. The

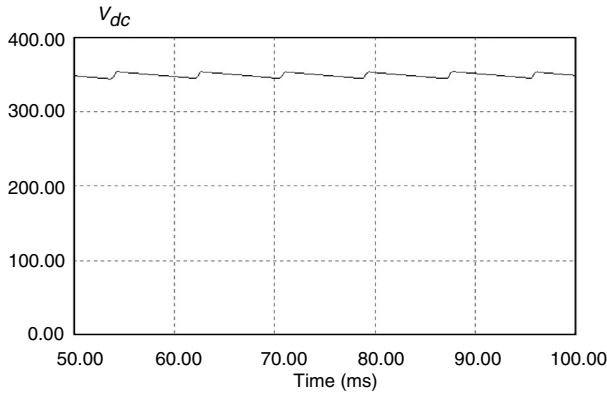


FIGURE 1.43
DC bus voltage for the controlled rectifier of Figure 1.41.

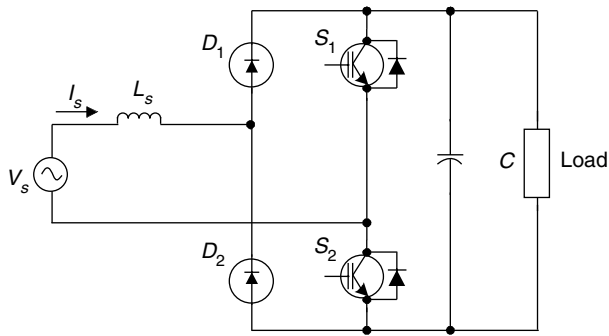


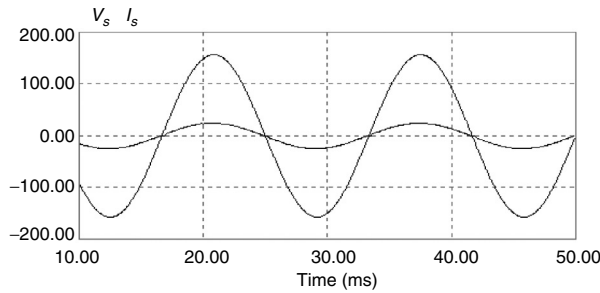
FIGURE 1.44
A full-bridge controlled rectifier with two active switches.

cost is lower because diodes are cheaper than IGBTs and because there is a cost related to the control of the IGBTs, that is, gate drivers and power supplies for the gate drivers. Although the control flexibility of this topology is more limited, the power factor can still be unity as shown in Figure 1.45. However, the input inductor L_s is larger than that of Figure 1.41.

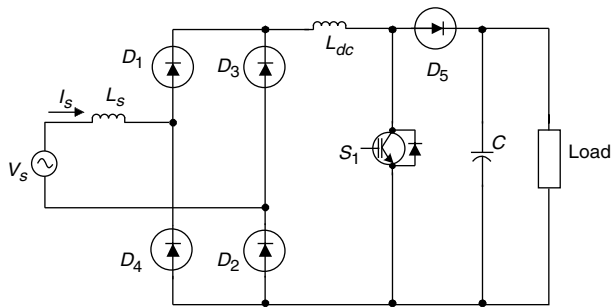
The concept of reducing the number of active switches can be expanded further as shown in Figure 1.46, where a full-bridge uncontrolled rectifier is connected in series with a boost converter. The boost converter consists of switch S_1 , inductor L_{dc} , and diode D_5 .

When the switch S_1 is closed, the current through the inductor L_{dc} increases. When it is open, the inductor current decreases. In this way, the input current is kept sinusoidal and in phase with the input voltage, as shown in Figure 1.47.

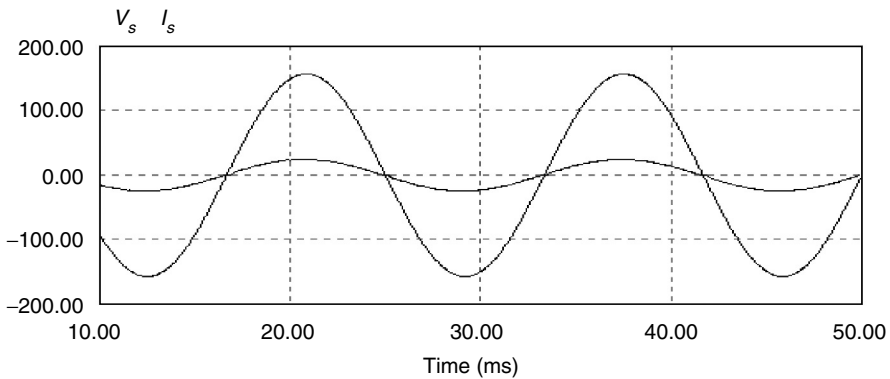
It should be mentioned here that the core of the current shaping inductor in this topology is larger in order to avoid saturation due to the fact that the inductor current is pure DC.

**FIGURE 1.45**

Input source current and voltage for the controlled rectifier of Figure 1.44.

**FIGURE 1.46**

A full-bridge AC/DC rectifier with boost DC/DC converter.

**FIGURE 1.47**

Input source current and voltage for the controlled rectifier of Figure 1.46.

The controlled voltage-doubler is shown in Figure 1.48.

During the positive half cycle, when the switch S_2 is on, the inductor current increases, and, when S_2 is off, the current decreases. In this way, S_2 shapes the input current during the positive half cycle. Accordingly, S_1 shapes the input current during the negative half cycle of V_s .

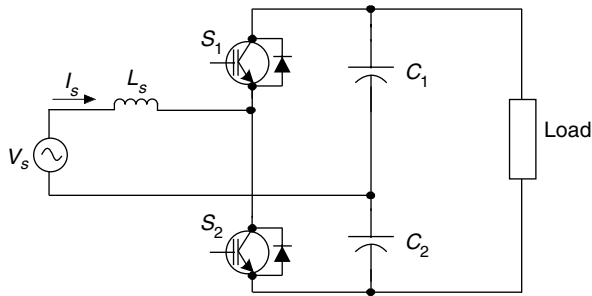


FIGURE 1.48
A controlled voltage-doubler rectifier.

1.10.2 Inverters

1.10.2.1 Basic Principles of Operation

There are two types of single-phase inverters: half-bridge inverter and full-bridge inverter [16]. A typical half-bridge inverter topology is shown in Figure 1.49. The split DC bus consists of two equal DC capacitors, C_1 and C_2 , connected in series and two switches (IGBTs), S_1 and S_2 , connected in series. The input DC voltage (V_{dc}) is equally divided between the two capacitors. By turning on and off switches S_1 and S_2 , the voltage applied across the load can be $+V_{dc}/2$ or $-V_{dc}/2$. When switch S_1 is on, switch S_2 is off and the load voltage is $+V_{dc}/2$. Also, when switch S_2 is on, switch S_1 is off and the load voltage is $-V_{dc}/2$. To avoid shoot-through faults, there is always a dead band between the time when one of the switches is turned off and the other is turned on. The duration of the dead band should be large enough to allow the switch that is turned off to close before the other switch, to start conducting. The advantages of the half-bridge inverter topology are a lower

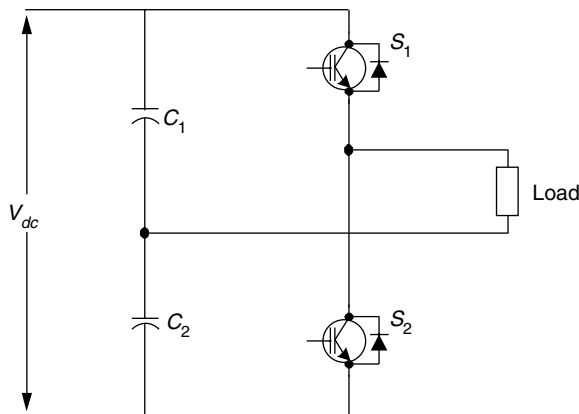


FIGURE 1.49
Half-bridge single-phase DC/AC inverter.

number of switches and simple control. However, it suffers from two main inherent disadvantages. The first one is poor utilization of the input DC voltage. The second one is that only bipolar PWM switching schemes can be applied with this topology. This inherently requires a larger output filter and generally leads to lower efficiency.

Because of the above mentioned disadvantages, the use of the half-bridge inverter topology is limited to the low-power applications. For medium- and high-power applications, the full-bridge inverter topology is usually used [71]. A typical full-bridge inverter topology is shown in Figure 1.50.

The full-bridge inverter consists of DC capacitor C and four switches (IGBTs), S_1 , S_2 , S_3 , and S_4 , connected in series two-by-two in two inverter legs. By turning on and off the switches, the voltage applied across the load can be $+V_{dc}$, $-V_{dc}$, or 0. When switches S_1 and S_2 are on, switches S_3 and S_4 are off and the load voltage is $+V_{dc}$. When switches S_3 and S_4 are on, switches S_1 and S_2 are off and the load voltage is $-V_{dc}$. In addition, when switches S_1 and S_3 are on, switches S_2 and S_4 are off and the load voltage is 0. Similarly, when switches S_2 and S_4 are on, switches S_1 and S_3 are off and, accordingly, the load voltage is 0. Again, to avoid shoot-through faults, there is always a dead band between the time when one of the switches in an inverter leg is turned off and the other is turned on.

1.10.2.2 Pulse Width-Modulated Switching Scheme

In PWM switching schemes, the output voltage is directly proportional to the duty cycle of the switches and the amplitude of the DC bus voltage V_{dc} . The output voltage can range from $-V_{dc}$ to $+V_{dc}$. Since the amplitude of the input DC voltage is usually fixed, the only way to shape the output voltage is to control the duty cycle of the switches. In order to do so, in the case of a PWM technique, a sinusoidal reference signal oscillating at the desired frequency is compared with a high-frequency triangular carrier waveform, as

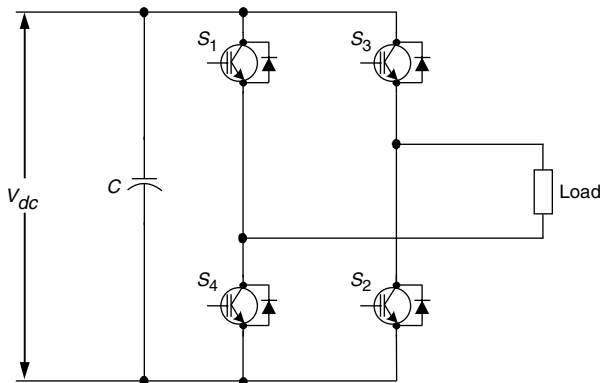


FIGURE 1.50
Full-bridge single-phase DC/AC inverter.

shown in Figure 1.51. This PWM technique is basically known as the bipolar switching scheme. The frequency of the triangular carrier waveform determines the inverter switching frequency and is generally kept constant at an amplitude of V_{tri} [71].

It is necessary to introduce a few terms before the discussion on the PWM technique. The triangular waveform, V_{tri} , in Figure 1.51, basically oscillates at the switching frequency f_s . It is this frequency that decides the frequency at which the inverter switches are turned on and off. On the other hand, the control signal, $V_{control}$, is used to modulate the switch duty

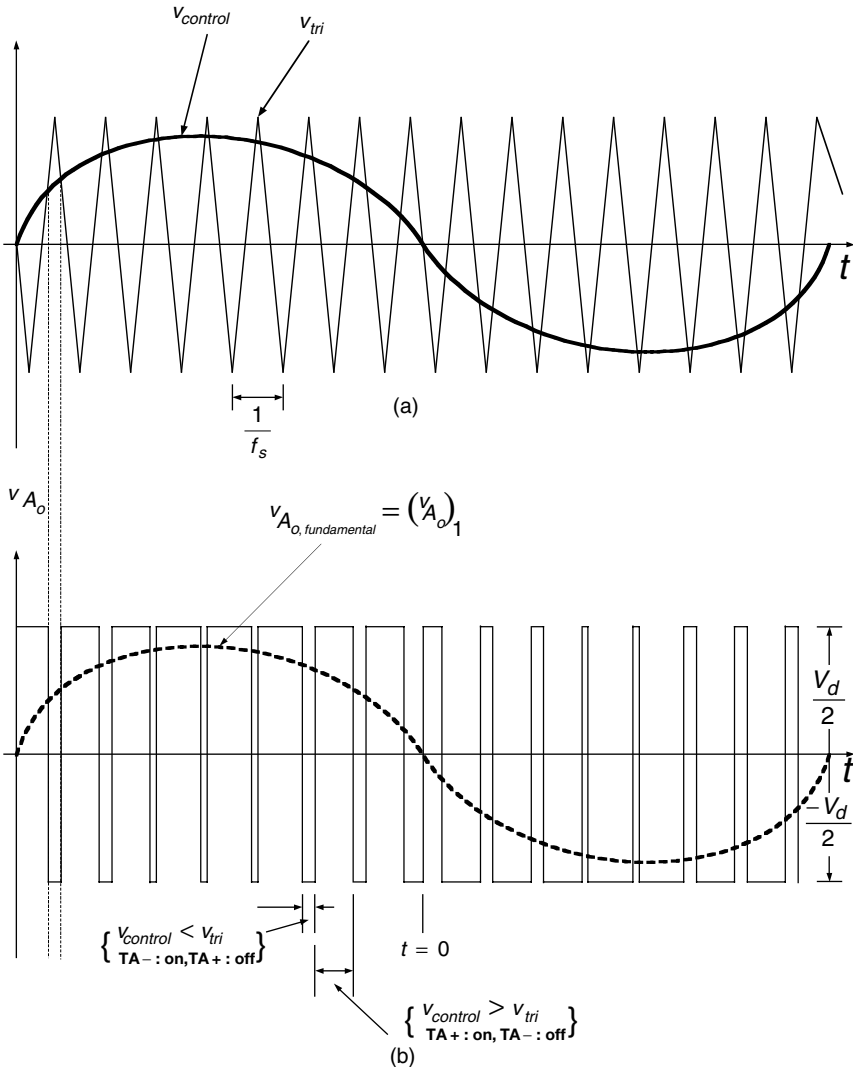


FIGURE 1.51

Diagrammatic representation of the bipolar PWM switching technique.

ratio and oscillates at the frequency of f_1 . This is basically the desired frequency at which the fundamental component of the output voltage oscillates. Furthermore, the output voltage as mentioned earlier is not a pure sinusoidal waveform and consists of voltage components oscillating at harmonic frequencies of f_1 [71].

From Figure 1.51, the important terms of amplitude and frequency modulation ratios can be defined. The amplitude modulation ratio, m_a , is defined as follows:

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \quad (1.12)$$

Here, $V_{control}$ is the peak amplitude of the control signal, whereas V_{tri} is the peak amplitude of the triangular carrier signal and is generally maintained constant. The value of the ratio m_a is generally less than 1. Therefore, the amplitude of the fundamental frequency component is linearly dependent on the amplitude of the modulation index.

Referring back to Figure 1.51, the frequency modulation ratio m_f can be defined as follows:

$$m_f = \frac{f_s}{f_1} \quad (1.13)$$

In the full-bridge DC/AC inverter of Figure 1.50, the switches S_1 , S_2 , S_3 , and S_4 are controlled by comparing the magnitudes of $V_{control}$ and V_{tri} . The output voltage across the load may vary accordingly and is as follows:

$$v_{control} > v_{tri}, \quad S_1, S_2 : \text{ON} \quad \& \quad S_3, S_4 : \text{OFF}, \quad v_{Ao} = V_d/2 \quad (1.14)$$

$$v_{control} < v_{tri}, \quad S_3, S_4 : \text{ON} \quad \& \quad S_1, S_2 : \text{OFF}, \quad v_{Ao} = -V_d/2 \quad (1.15)$$

Thus, since the two switches are never off simultaneously, the output voltage V_A fluctuates between $V_d/2$ and $-V_d/2$ [17]. Another popular variation of the PWM technique as mentioned before is the unipolar switching scheme. The typical waveforms for this scheme are shown in Figure 1.52. They are generated from simulations [72].

The sine curve in Figure 1.52 is the control signal for switches S_1 and S_3 and has a phase angle of 0° . We name it $V_{control-1}$. The negative sine curve is the control signal for switches S_2 and S_4 and it is 180° phase-shifted from the first control signal. We name it $V_{control-2}$. As is clear from Figure 1.52, in the case of unipolar switching scheme for PWM, the output voltage is either switched from high to zero or from low to zero unlike in the bipolar switching scheme where the switching takes place directly between high and low [71]. As a result, the content of high-order harmonics in the output voltage is much lower compared to the corresponding one from the bipolar switching scheme. Consequently, the required output filter can be considerably smaller and the overall efficiency of the system is higher. Referring back to Figure 1.50, the full-bridge DC/AC inverter can have the following switch controls under unipolar PWM switching scheme:

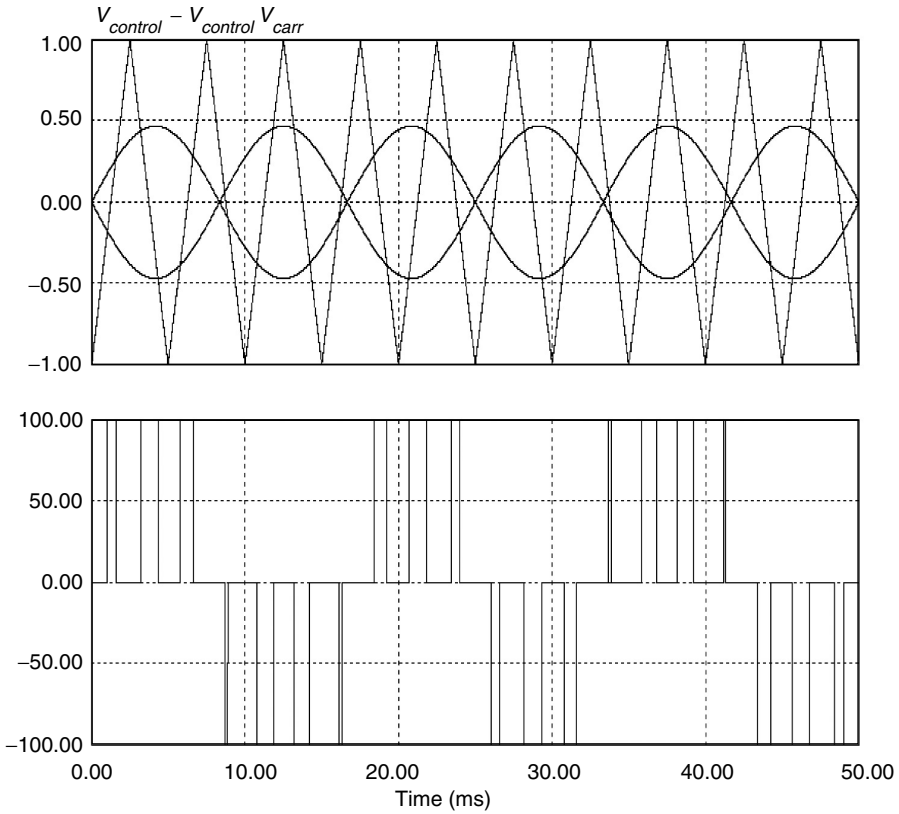


FIGURE 1.52
Unipolar PWM switching technique.

$$V_{control_1} > V_{tri} \quad S_1 \text{ is on; } S_4 \text{ is off} \quad (1.16)$$

$$V_{control_1} < V_{tri} \quad S_4 \text{ is on; } S_1 \text{ is off} \quad (1.17)$$

$$V_{control_2} > V_{tri} \quad S_3 \text{ is on; } S_2 \text{ is off} \quad (1.18)$$

$$V_{control_2} < V_{tri} \quad S_2 \text{ is on; } S_3 \text{ is off} \quad (1.19)$$

The switch pairs S_1/S_4 and S_2/S_3 are complementary to each other. When one of the switch pairs is on, the other switch pair must be off.

1.11 Battery Charger/Discharger

Batteries are among the most important components in the UPS systems. No matter how good the design of the power electronic circuits is, if batteries fail

to operate properly, the whole UPS system fails to fulfill its purpose. In fact, batteries are the weakest component in the UPS systems. They are extremely sensitive to nonoptimal operating conditions such as high or low temperature, deep discharge, and overcharge.

While ambient temperature is not in the control of the UPS designer and very little can be done with regard to this, in the sense of temperature compensation, control of charging and discharging of batteries are of main concern in the UPS system design process.

There are two options for connecting batteries in the UPS systems. The first one is to connect them directly in parallel with the DC bus capacitors as shown in Figure 1.53.

This configuration results in a very simple system. The controlled rectifier itself serves as a charger for the batteries by maintaining an appropriate DC bus voltage. However, many battery cells need to be connected in series to maintain a high DC bus voltage. This requirement leads to several problems such as space, cost, reliability, and safety. Space limitations and cost considerations are critical design parameters in the low-power UPS applications such as personal computers. The safety problem with regard to maintaining high voltage at the battery terminals leads to a higher maintenance cost. High voltage requires a trained staff for monitoring and replacement of batteries while low voltage allows nontrained staff to do the same job. Reliability is also an issue in a high-voltage battery bank. For a certain storage capacitance, the reliability decreases as the number of battery cells connected in series increases.

Among the different solutions that have been proposed to overcome the high-voltage battery problems, the most popular one is to add a bidirectional DC/DC converter. It steps down the high DC bus voltage to the low battery voltage during the charging mode of operation and steps up the low battery voltage to the high DC bus voltage during the backup mode of operation. A typical bidirectional DC/DC converter employed in an on-line UPS system is shown in Figure 1.54. Figure 1.55 shows the bidirectional DC/DC converter itself.

The buck converter consists of switch S_2 , diode D_1 , and inductor L_{dc} . Switch S_2 chops the high voltage V_{dc} and steps it down to $V_{bat} = DV_{dc}$, where D is the duty ratio of switch S_2 . The boost converter consists of switch S_1 , diode D_2 , and inductor L_{dc} . When S_1 is closed, inductor L_{dc} is energized. When S_1 is opened, the energy stored in L_{dc} is transferred to the output stepping up the low battery voltage V_{bat} to the high DC bus voltage $V_{dc} = V_{bat}/(1-D)$ where D is the duty ratio of switch S_1 .

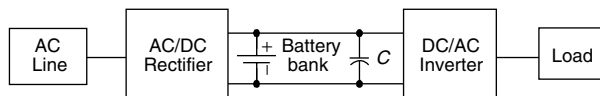
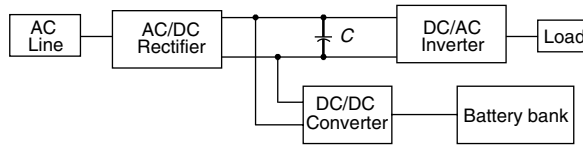
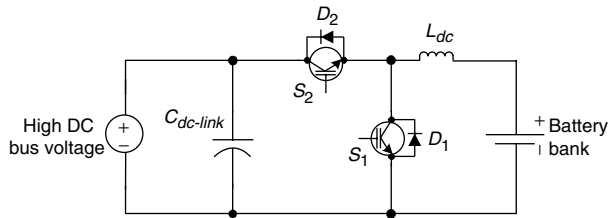


FIGURE 1.53

UPS system with a battery bank directly connected to the DC-link bus.

**FIGURE 1.54**

UPS system with a battery bank connected to the DC-link bus through a bidirectional DC/DC converter.

**FIGURE 1.55**

A bidirectional buck-boost DC/DC converter.

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2

Active Filters

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In recent years, with the increase of nonlinear loads drawing nonsinusoidal currents, power quality distortion has become a serious problem in electrical power systems. Active filters have been known as the best tool for harmonic mitigation as well as reactive power compensation, load balancing, voltage regulation, and voltage flicker compensation. This chapter describes

harmonic producing loads, effects of harmonics, and harmonic mitigation methods, especially using active filters. Different topologies of active filters, their applications, configurations, control methods, modeling and analysis, and stability issues are also discussed in this chapter.

2.1 Harmonic Definition

Harmonic is defined as “a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency” [1]. Therefore, harmonic is the presence of voltage/current with the frequency of a multiple of fundamental voltage/current in the voltage/current of the system. For example, Figure 2.1 shows a waveform with 60 Hz fundamental frequency and fifth (300 Hz), seventh (420 Hz), eleventh (660 Hz), and thirteenth (780 Hz) harmonics.

For the metering and comparison of harmonic contents of waveforms, a parameter is defined as a total harmonic distortion (THD). THD is defined for both current and voltage as follows [2]:

$$\text{For voltage: } THD_v = 100 \frac{\sqrt{V_h^2}}{V_1} \quad (2.1)$$

$$\text{For current: } THD_i = 100 \frac{\sqrt{I_h^2}}{I_1} \quad (2.2)$$

where I_h and V_h are current and voltage harmonics, respectively.

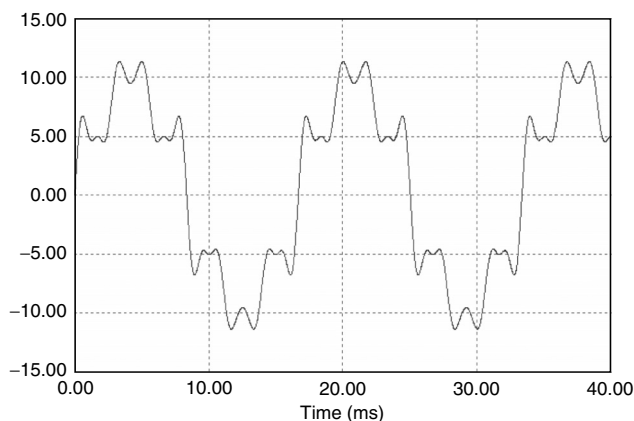


FIGURE 2.1

A sample waveform including harmonics.

2.2 Harmonic Sources in Electrical Systems

There are many nonlinear loads drawing nonsinusoidal currents from electrical power systems. These nonsinusoidal currents pass through different impedances in the power systems and produce voltage harmonics. These voltage harmonics propagate in power systems and affect all of the power system components. These harmonic sources are classified as follows.

2.2.1 Fluorescent Lamps

Figure 2.2 shows the input current of a typical fluorescent lamp. The amount of harmonics no. 3, 5, 7, and nine are high. Liew’s experimental results [3] show the maximum and minimum harmonic contents of a fluorescent lamp, as presented in Table 2.1.

A detailed experimental investigation of the harmonic distortion and power factor of energy-efficient lamps is presented by Etezadi-Amoli and Florence [4].

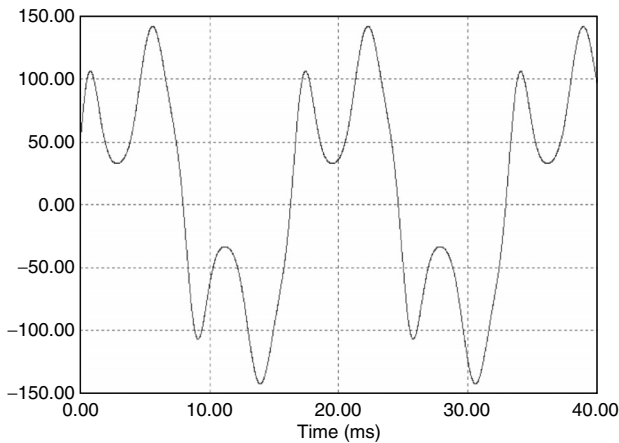


FIGURE 2.2
Input current of a typical fluorescent lamp.

TABLE 2.1
Maximum and minimum harmonic contents of a typical
fluorescent lamp current

Harmonic no.	Max (%)	Min (%)
1	100	100
3	63.4	42.9
5	8.9	8.3
7	10.4	6.4
9	3.0	.56

2.2.2 Switching Power Supplies

Figure 2.3 shows a typical input current of a computer power supply and its harmonic spectrum. Other small electronic devices such as televisions, air conditioners, laser printers, and Xerox machines have similar input current waveforms.

Although the input current and power of these systems are small compared to the power system devices, they are used extensively and can be found everywhere; therefore, the sum of their harmonics results in a high harmonic distortion in line currents [5].

2.2.3 Electric Furnace

The electric furnace is one of the high-power and high harmonic distortion devices in electrical power systems. In fact, when a furnace is melting a new steel scrap, its current is not periodic and even possesses noninteger order of harmonics [2]. Figure 2.4 shows the input current of a typical electric furnace and its harmonic spectrum. High fifth and seventh harmonics cause high distortion in input current [6]. Therefore, harmonic mitigation devices are used at the input side of these systems.

2.2.4 High-Voltage DC Systems

High-voltage DC (HVDC) systems are used for long-distance high-power transmission. Usually, in HVDC systems, 12-pulse rectifiers are used for AC/DC conversion. By using a 12-pulse inverter, in AC side, we have harmonics of order 12 ± 1 ($n=1, 2, 3, \dots$). The main harmonic components are of the order of 11 and 13. Table 2.2 shows the current harmonic content in the AC side at Dickinson of the ± 400 KV, 1000MW CU HVDC transmission system [7].

The AC side current waveform of a typical HVDC system and its harmonic spectrum are shown in Figure 2.5.

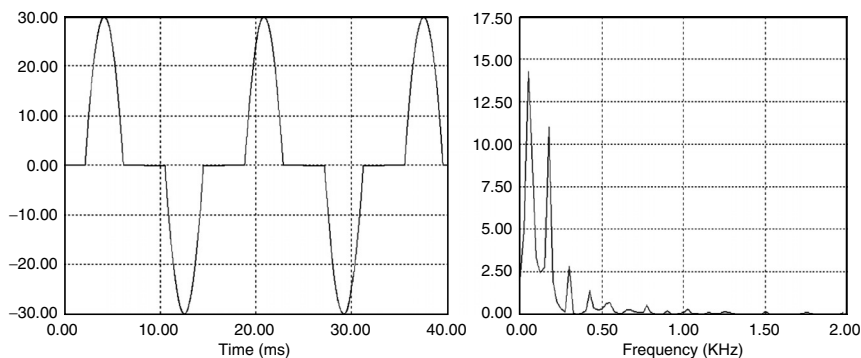


FIGURE 2.3

Input current of a typical computer power supply and its harmonic spectrum.

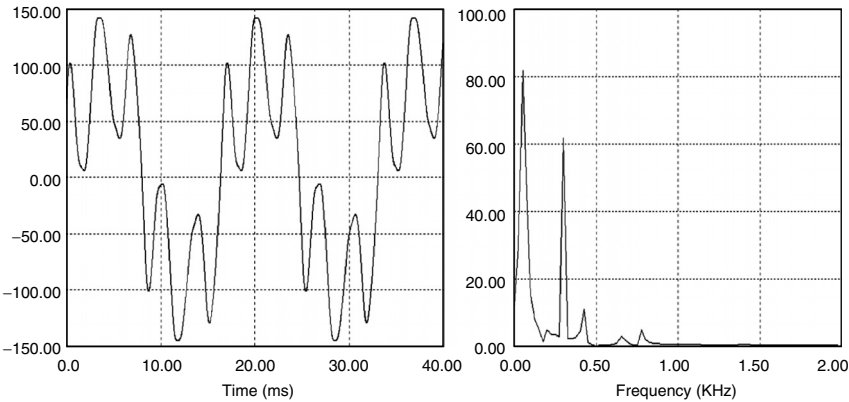


FIGURE 2.4
Input current and its harmonic spectrum of a typical electric furnace.

TABLE 2.2
Current harmonic content of the Dickinson HVDC system

Harmonic order	11	13	23	25	35	37	47	49
Current (A)	119	70	18	13	7	6	4	4

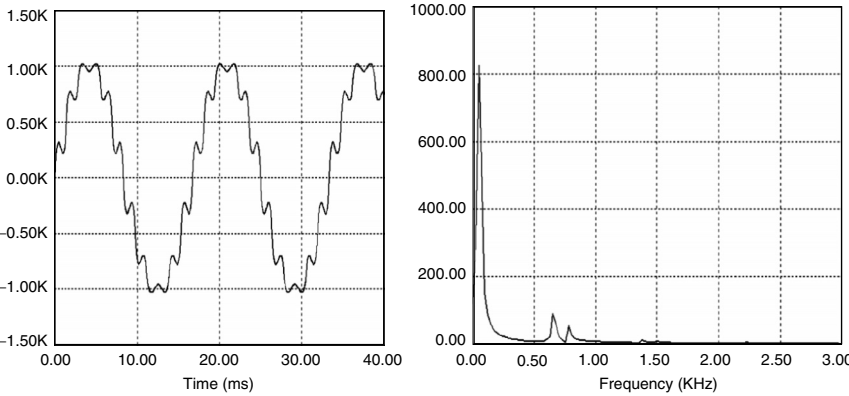
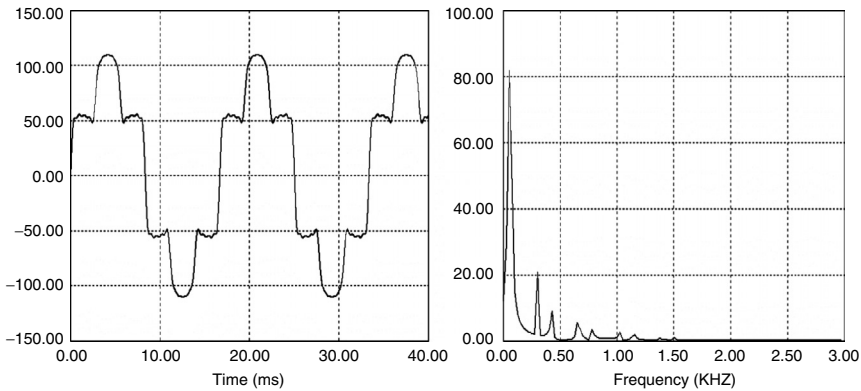


FIGURE 2.5
AC side current of a typical HVDC system and its harmonic spectrum.

At the DC side, there are harmonics of the order of $12n$ ($n=1, 2, 3\dots$). Their amplitudes are also considerably high.

2.2.5 Adjustable Speed Drives

With the increase of adjustable speed drives (ASD) in electrical power systems, they have become a main problem for power quality. [Figure 2.6](#) shows

**FIGURE 2.6**

Input current and harmonic spectrum of a typical ASD.

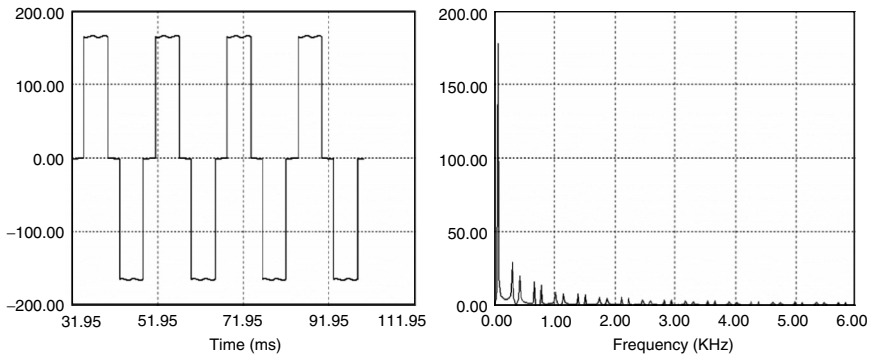
the input current of a typical ASD and its harmonic spectrum. The harmonics of order 5 and 7 are considerably high [8].

2.2.6 AC/DC Converters/Inverters

Many low-power single-phase converters/inverters and high-power three-phase converters/inverters are being used in electrical power systems. If the number of converter/inverter pulses is p , then the order of harmonic current in AC side will be $np \pm 1$ ($n=1, 2, 3\dots$). Figure 2.7 shows the input current of a typical 6-pulse converter and its harmonic spectrum.

2.2.7 Other Harmonic-Producing Loads

Almost every device that uses power electronic components such as renewable electrical power generation systems, cycloconverters, electronic

**FIGURE 2.7**

Input current of a typical 6-pulse AC/DC converter and its harmonic spectrum.

phase control loads, and pulse width modulation (PWM) drives produce harmonics.

2.3 Effects of Harmonics

Except devices such as ovens and furnaces, which produce heat, most of the other electrical loads are sensitive to harmonics. In fact, harmonics may lead to their improper operation. The effects of harmonics in power systems and electrical loads are described below.

2.3.1 Disturbance to Electric and Electronic Devices

Passing harmonic currents through the transmission lines causes interference with the communication circuits near the transmission lines and may cause a malfunction in these circuits. On the other hand, harmonics cause disturbance in sensitive loads in power systems such as sensitive medical devices, control circuits, and computers [9].

Control circuits that work on current or voltage zero crossing have higher sensitivity to harmonics and may not work properly in the presence of harmonics. Figure 2.8 shows how harmonics cause disturbance in these loads. The zero crossings are five times more than the situation without harmonics.

2.3.2 Higher Losses

The loss in the power transmission lines can be expressed as

$$P_{Loss} = RI^2 \quad (2.3)$$

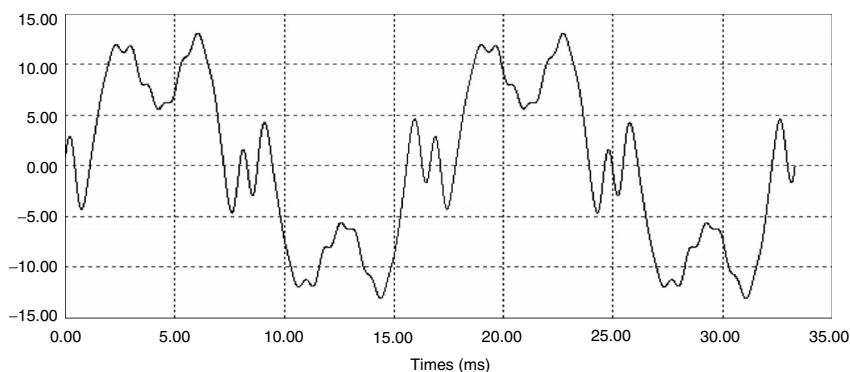


FIGURE 2.8

Effect of harmonics on zero passing controllers.

where R is the AC resistance of the transmission line and I is the RMS value of the line current. If the current includes harmonics, we have

$$I_2 = I_1^2 + \sum I_h^2 \quad (2.4)$$

and then

$$P_{Loss-h} = R \sum I_h^2 \quad (2.5)$$

Although the harmonic currents cannot apply active power to the loads, they cause higher losses in the transmission lines. Harmonics also cause higher losses in power transformers, which are proportional to the square of the harmonic amplitude.

Excessive losses and torque fluctuation also appear in electric motors in the presence of harmonics because only the fundamental component yields average torque in motors and harmonics yield core losses and torque fluctuation [6].

2.3.3 Extra Neutral Current

The presence of current harmonics in electrical power systems increases neutral currents. In this case, the most important part of the neutral current is the third harmonic. Liew's experimental results [3] show that in fluorescent lamp circuits, the neutral current is 30% of the line current. In other nonlinear loads such as adjustable speed drives, this percentage is higher. Harmonic current components and neutral currents of a typical computer power supply are shown in Table 2.3 [5].

Table 2.3 shows that the amount of neutral current is 1.61 times greater than the amount of the phase current.

Higher neutral currents, in four-wire, three-phase systems, in addition to the increasing size of the neutral wire, can cause overloaded power feeders, overloaded transformers, voltage distortion, and common mode noise.

2.3.4 Improper Working of Metering Devices

The presence of current and voltage harmonics of more than 5% may lead to improper working of conventional metering devices that utilize induction watt-hour meters [10].

TABLE 2.3

Harmonics and neutral currents of a typical computer power supply

Harmonic order	1	3	5	7	9	11	13	Total phase current	Neutral current	Ratio of neutral to phase current
Current harmonic (A)	.65	.52	.42	.29	.13	.12	.098	1.00	1.61	1.61

2.3.5 De-Rating of Distribution Equipment

The presence of harmonics increases the RMS value of the phase and neutral currents. Therefore, thicker wires are needed in the presence of harmonics. The distribution transformers are also de-rated. ANSI/IEEE C57.110-1986 standards recommend the following equation for the de-rating of a transformer with a power rating between 15 and 225 KVA:

$$De\text{-}rating = \sqrt{\frac{1 + P_{EC-R}}{1 + (\sum I_h^2 / \sum I_h^2) P_{EC-R}}} \quad (2.6)$$

where P_{EC-R} is the eddy current loss at the rated power [11].

2.3.6 Resonance Problem

One of the problems caused by harmonics is resonance in power circuits. Current and voltage harmonics, which are produced by nonlinear loads, when passing through the power system or another load, may cause a resonance problem. Figure 2.9 shows a kind of resonance where the load has a resonance frequency close to the fifth harmonic. When there is a small amount of fifth harmonic in line voltage, the eleventh harmonic current drawn by the load is too high.

2.4 Harmonic Mitigation Methods

Mitigation or cancellation of harmonics can be done by using passive or active filters. However, it is better to prevent harmonics in production.

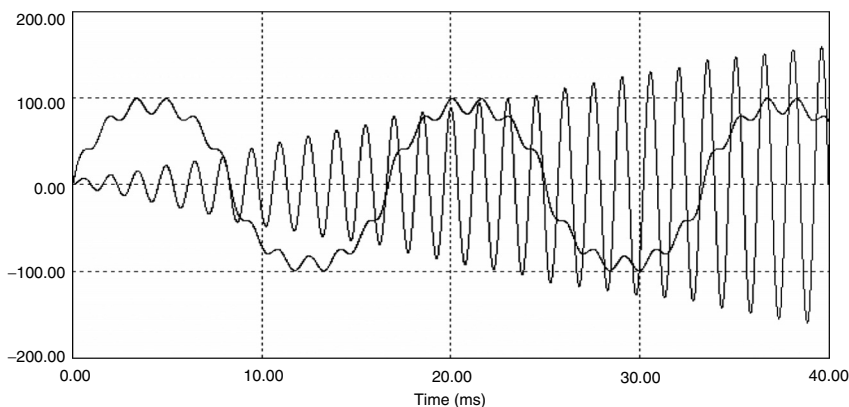


FIGURE 2.9

Resonance because of a resonance frequency near the fifth harmonic.

2.4.1 Harmonic Production Prevention

Changing and improving the characteristics of nonlinear devices can reduce the amount of produced harmonics. Improvements can be made in the two most harmonic-producing loads: converter/inverter systems and DC power supplies. Reduction of harmonic amplitude and low-frequency harmonic cancellation can be done with increasing pulse in the converter/inverter systems. By changing the 6-pulse inverter to 12-pulse, harmonics of order 5 and 7 are canceled. Improving the DC power supply topology and control scheme improves the input current's harmonic spectrum. The use of boost, Cuk, single-ended primary inductor converter (SEPIC), and boost-integrated flyback rectifier/energy storage DC/DC (BIFRED) choppers instead of buck, buck-boost, flyback, and forward converters may improve the quality of the input current [12]. [Figure 2.10](#) shows the input current of buck, boost, and BIFRED DC/DC converters and their harmonic spectra.

2.4.2 Passive Filters

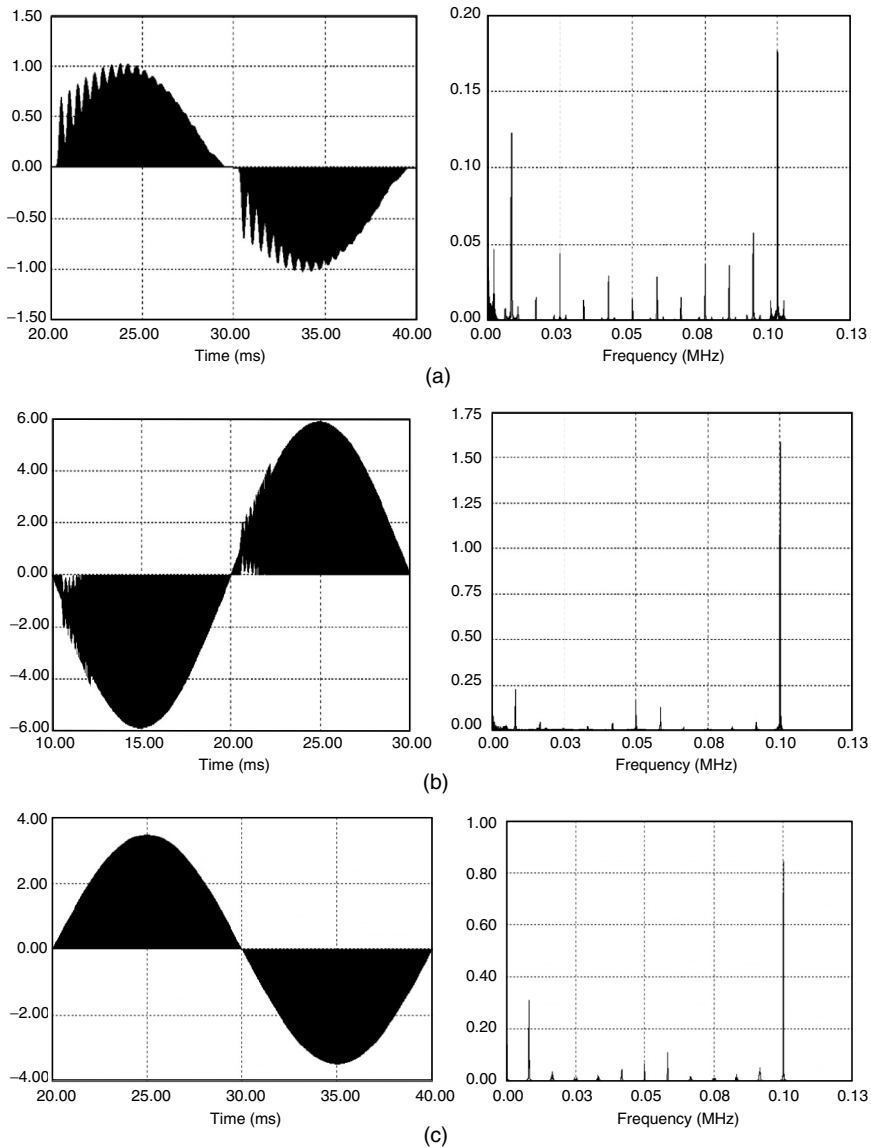
Passive filters have been used for harmonic mitigation purposes for a long time. They consist of capacitors, inductors, and damping resistors. Passive filters, based on their characteristics, are divided into four categories: low-pass, band-pass, high-pass, and tuned filters. [Figure 2.11](#) shows the frequency response of these four types of passive filters. Low- and high-pass filters cancel the high- and low-order harmonics, respectively. A band-pass filter (BPF) cancels the high- and low-order harmonics and passes a band of frequency. The tuned filter is designed to cancel one specific frequency.

The increased severity of power quality problems and other problems associated with the passive filters such as large size and weight, higher cost, fixed compensation, and resonance problems with loads and networks have required a focus on a power electronic solution, that is, active filters. Nowadays, passive filters are used to cancel the switching frequency of active filters and high frequencies [13, 14]. Tuned filters are used besides the active filters to cancel specific frequencies and decrease the power of active filters.

2.4.3 Active Filters

Active filters have been designed, improved, and commercialized in the past three decades. They are applicable to compensate current-based distortions such as current harmonics, reactive power, and neutral current. They are also used for voltage-based distortions such as voltage harmonics, voltage flickers, voltage sags and swells, and voltage imbalances.

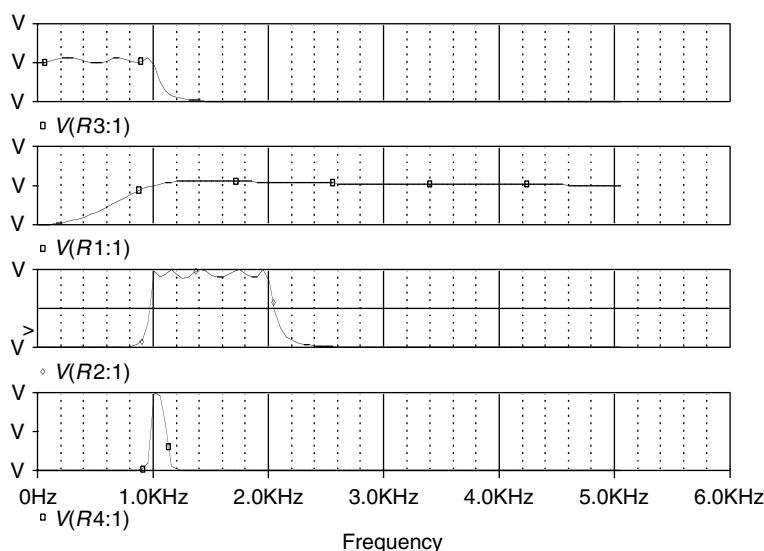
Active filters are categorized into two main groups: single-phase and three-phase. Three-phase active filters may be with or without neutral connection. Single-phase active filters are used to compensate power quality

**FIGURE 2.10**

Input current and harmonic spectrum of (a) buck, (b) boost, and (c) BIFRED converters.

problems caused by single-phase loads such as DC power supplies. Three-phase active filters are used for high-power nonlinear loads such as adjustable speed drives and AC/DC converters.

An active filter can utilize current source inverters (CSIs) or voltage source inverters (VSIs). CSI-based active filters employ an inductor as the energy storage device. VSI-based active filters use a capacitor as the energy

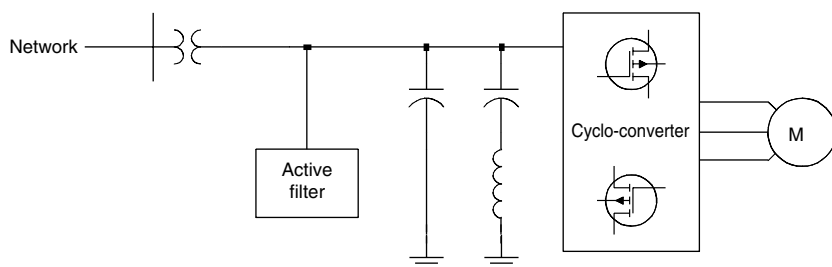
**FIGURE 2.11**

Frequency response of low-pass, high-pass, band-pass, and tuned filters (from top to bottom).

storage device. Many configurations such as shunt, series, hybrid (a combination of shunt and series active filters), and unified power quality conditioner (UPQC), which is a combination of series and shunt active filters, have been introduced and improved. Many control techniques such as the instantaneous $p-q$ theory, the synchronous $d-q$ reference frame method, the synchronous detection method, notch filter, $P-I$ method, sliding mode control, and the frequency domain method have been introduced and applied to various configurations of active filters [15]. Details are discussed in this chapter.

2.4.3.1 Applications

Active filters have been designed and developed for compensation of current and voltage harmonics; yet, now they have many functions and many applications. Active filters, based on topology and control scheme, can compensate current harmonics, voltage harmonics, reactive power, load imbalance, neutral current, voltage imbalance, voltage regulation, voltage flicker, and voltage sag and swell. As mentioned before, active filters are installed near the high-power nonlinear loads such as electric furnaces, HVDC systems, and ASDs to compensate the effects of their nonlinearity on the power networks. In this section, some special applications of active filters are explained. In variable-speed cycloconverter drive systems, active filters are used in the AC side to reduce the variable frequency current harmonics, which are produced by both the converter and inverter as shown in Figure 2.12 [16]. Passive filters cannot work properly because the frequency is variable.

**FIGURE 2.12**

Application of an active filter with a cycloconverter.

2.4.3.1.1 Adjustable Speed Drives

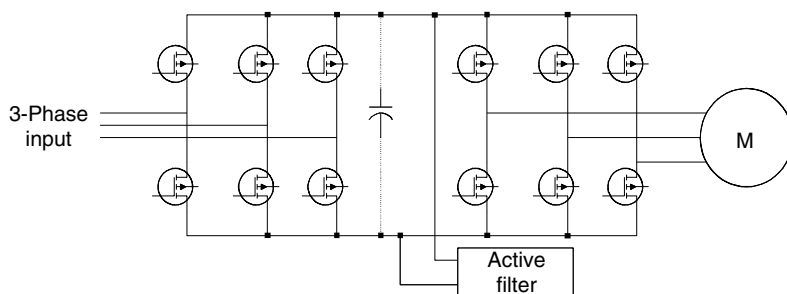
In induction motor drives, there is an interference between the harmonic and signaling system, leading to improper working of the system. Simple low-pass passive filters can be used to suppress these harmonics; however, they will be large and heavy. For example, a low-pass LC passive filter with a corner frequency of 5 kHz for an induction motor of 1.5 MW has a total weight of 5 tons [17].

2.4.3.1.2 DC Capacitor Cancellation

Another application of active filters, is the cancellation of bulky and unreliable capacitors with a current-fed small size, reliable, costly, and resonance-free shunt active filter [18], as shown in Figure 2.13. This active filter cancels voltage harmonics in the DC-link of the DC/AC converter and makes the voltage of this DC-link smooth; therefore, the quality of the output AC will be better.

2.4.3.1.3 HVDC Systems

Active filters are used in both DC and AC sides of the HVDC systems to cancel the voltage harmonics in the DC side and current harmonics in the

**FIGURE 2.13**

Cancellation of a capacitor in DC/AC converter.

AC side [19]. Orders of voltage harmonics in the DC side are of $12n$ ($n=1, 2, 3, \dots$) and orders of current harmonics in the AC side are $12n \pm 1$ ($n=1, 2, 3, \dots$).

2.4.3.1.4 High-Power Locomotives

In high-power locomotives, current harmonics produced by variable-frequency DC/AC inverters cause excessive losses in AC/DC converters (Figure 2.14) and transformers. Active filters offer the best choice to mitigate these harmonics [20].

2.4.3.1.5 Remote Generations

Remote generation circuits have a higher efficiency when working with variable frequency. Current harmonics caused by the nonlinear loads in these systems cause higher losses in the generator and distortion in voltage, which cannot be mitigated by passive filters [21]. In a typical wind power generation circuit, when it is connected to a power network, active filters should be used to prevent harmonics from flowing into the power system [22].

2.4.3.1.6 Commercial Loads

Commercial buildings, wherein many nonlinear loads such as computers, laser printers, fluorescent lights, and other electronic equipment are used, can benefit from active filters to compensate current harmonics, reactive current, neutral current, and load imbalance. Active filters can also prevent the effect of the voltage harmonic and voltage sag and swell from the network on loads.

2.4.3.1.7 Other Applications

Suppression of voltage flicker in arc furnace systems can be done by using high-frequency power active filters [23]. Another application is current harmonic compensation in magneto-hydrodynamic power generation systems [24]. A high precision DC magnet, which is used for particle acceleration, needs a well regulated DC current input. This current can be achieved by using a shunt power active filter [25].

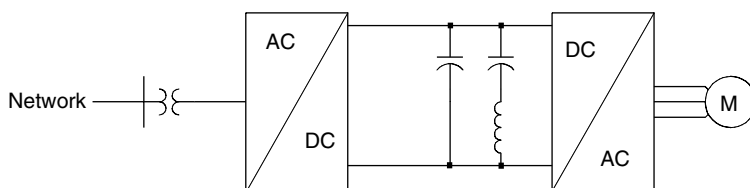


FIGURE 2.14

Variable-speed high-power induction motor for a locomotive.

2.5 Classification of Active Filters

Based on topology, there are two kinds of active filters: current source and voltage source active filters. Current source active filters (CSAFs) employ an inductor as the DC energy storage device. In voltage source active filters (VSAFs), a capacitor acts as the energy storage element. VSAFs are less expensive, lighter, and easier to control compared to CSAFs.

2.5.1 Current Source Active Filters

Nonlinear loads draw nonsinusoidal currents. These currents pass through the AC source impedance and spread voltage harmonics in the AC systems. Active filters are designed to generate the harmonic current equal to the harmonic current of the load. Therefore, the current of the AC source will be free of harmonics.

CSAFs use a current source as the DC energy storage device. They can be low-power, single-phase or high-power, three-phase three- or four-wire systems. Figure 2.15 shows the configuration of a three-phase, three-wire CSAF. R_s , L_s , R_l , L_l , R_f , and L_f are the resistance and inductance of the AC source, load, and filter sides, respectively.

Different kinds of control strategies have been introduced and improved for controlling the CSAF filter [26, 27]. The PWM current control method is the most popular control technique.

One of the three upper switches and one of the three lower switches must always be on simultaneously as shown in Figure 2.15. In three-phase, three-wire systems, we have

$$i_{sa} + i_{sb} + i_{sc} = 0 \quad (2.7)$$

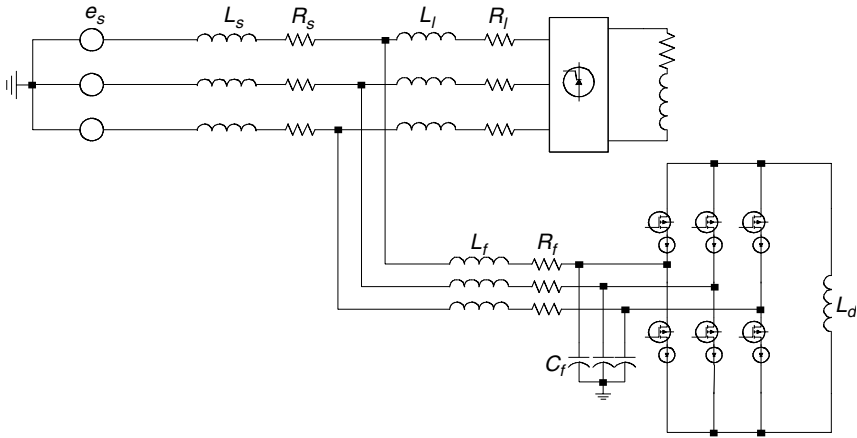
$$i_{sa}^* + i_{sb}^* + i_{sc}^* = 0 \quad (2.8)$$

where i_{sa} is the current of phase (a) at the source side and i_{sa}^* is the reference current. By subtracting these two equations, we have

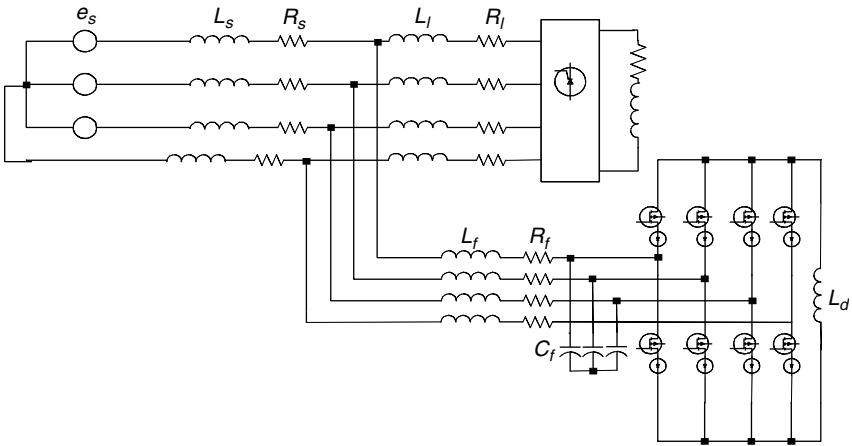
$$\Delta i_{sa} + \Delta i_{sb} + \Delta i_{sc} = 0 \quad (2.9)$$

Equation 2.9 implies that Δi_{sa} , Δi_{sb} , and Δi_{sc} do not have the same sign. In fact, one of them has a maximum positive magnitude and another one has a maximum negative magnitude [26]. The control system must pass the inductor current through the two phases, which have maximum positive and negative deviations. When there is no deviation in source current from the reference current, both the switches in one leg must be turned on. This state is called the short-through period.

In the three-phase, four-wire system (Figure 2.16), load current imbalance can be compensated with one switch of the phase leg and one switch of the null leg.

**FIGURE 2.15**

A typical three-phase current source active filter.

**FIGURE 2.16**

A typical three-phase, four-wire current source active filter.

In CSAFs, DC current of the energy storage inductor must be greater than the maximum harmonic of the load (maximum deviation of the source current from the reference value). If the current of the DC inductor (I_{dc}) is too small, the inverter cannot perform proper compensation. I_{dc} should not be too high, if it is, excessive loss exists in L_{dc} and inverter and passive filters cannot cancel the switching frequency [28]. There is no need for the DC power supply because the active filter delivers only reactive power and a small value of the fundamental current needed to compensate the active filter losses.

C_f is used to protect the switches against the overvoltages and also to make the LC low-pass filter with L_f to suppress the switching frequency [29]. To

prevent resonance, the resonance frequency of L_f and C_f must be greater than the highest frequency of the harmonics and considerably less than the switching frequency. The control strategy must be well designed to prevent this resonance.

L_{dc} must be chosen large enough to limit the current ripple. Maximum of L_{dc} is limited by the volume, weight, and cost. In CSAFs, energy circulates between L_{dc} and the system. When the voltage across L_{dc} is positive, the current of L_{dc} decreases and when the voltage across L_{dc} is negative, the current of L_{dc} increases. This increase and decrease cause a ripple on current of L_{dc} . Suppose ΔI is the ripple of L_{dc} current. Then,

$$\Delta W_{L_{dc}} = \frac{1}{2} L_{dc} ((I_{dc} + \Delta I)^2 - (I_{dc} - \Delta I)^2) = 2\Delta I L_{dc} I_{dc} \quad (2.10)$$

where $\Delta W_{L_{dc}}$ is the variation of energy in L_{dc} [30, 31]. As a result, we have

$$L_{dc} = \frac{\Delta W_{L_{dc}}}{2\Delta I I_{dc}} \quad (2.11)$$

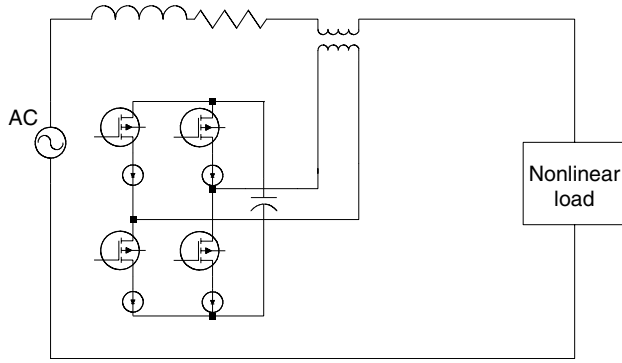
The cost of CSAF will be reasonable when high-temperature practical superconducting coils are available in the future [32].

2.5.2 Voltage Source Active Filters

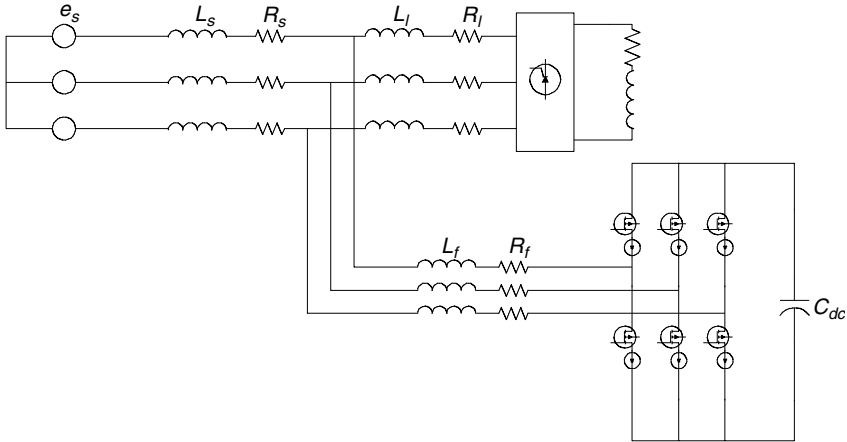
The most dominant type of active filter is the voltage source inverter-type active filter, which has been designed, improved, and used for many years and is now in the commercial stage. These filters are lighter, less expensive, and easier to control compared to the current source inverter type. Their losses are less than CSAFs and they can be used in multilevel and multistep configurations [15].

VSAFs use a capacitor as the DC energy storage. They are presented in single-phase or three-phase, three-wire or four-wire systems. This type of active filter is convenient in uninterruptible power supply (UPS) systems. In UPS systems, DC energy storage is available and the DC/AC inverter is also ready. A control strategy is only needed to convert the UPS into an active filter when the source is in normal condition. Figure 2.17 and Figure 2.18 show a single-phase and three-phase shunt VSAF. R_s , L_s , R_l , L_l , R_f , and L_f are the resistance and inductance of the AC source, load, and filter sides, respectively. Different kinds of control techniques are used to control VSAFs. These control techniques include instantaneous $p-q$ theory, synchronous $d-q$ reference frame method, and synchronous detection method, which will be discussed later [33].

In VSAFs, DC voltage of the energy storage capacitor must be greater than the maximum line voltage. For proper operation of the active filter, at any instant, the voltage of the DC capacitor should be 1.5 times that of the line maximum voltage [34]. When three-phase shunt VSAF compensates the current harmonics of a three-phase, six-pulse AC/DC rectifier, for controllability

**FIGURE 2.17**

A single-phase series voltage source active filter.

**FIGURE 2.18**

A three-phase shunt voltage source active filter.

of the active filter during the rectifier commutation V_C , the voltage of the DC capacitor can be found from the following equation [34]:

$$V_C \geq \sqrt{3}\pi V \sqrt{\cos(\alpha)^2 + [(k+1)\sin(\alpha) + \delta k]^2} \quad (2.12)$$

where

$$k = \frac{L_f}{L_s + L_l}, \quad \delta = \sqrt{6}(L_s - L_l) / \pi V \omega$$

and V is the RMS value of the line voltage.

L_f acts as a link between the filter and system. An active filter delivers its current to the system through the inductor. For controllability of the active filter, this inductor should not be large. On the other hand, L_f , as a first-order

passive filter, prevents switching frequency, which is generated by the inverter. Based on this feature, L_f should not be small. Therefore, a compromise should be made to find an appropriate value for L_f .

The DC capacitor, C_{dc} , should be large enough to limit the voltage ripple on this capacitor. For the controllability purposes, ripple on this capacitor should be small. In general, minimum of C_{dc} can be found from the following equation:

$$C_{dc} = \frac{P_h}{\omega V_C \Delta V_C} \quad (2.13)$$

where P_h is the maximum power of the harmonics, which must be delivered in each half-period, and ΔV_C is the peak-to-peak ripple of the capacitor voltage.

2.5.3 Shunt Active Filters

The most popular type of active filters is the shunt active filter. Shunt active filters can be single-phase or three-phase, voltage source or current source. Figure 2.19 shows the equivalent circuit of a shunt active filter, source, and load when the filter is used to compensate the current and voltage harmonics [35]. In Figure 2.19(a), the active filter compensates the harmonic current of a nonlinear load, which produces harmonic current. Figure 2.19(b) shows that the shunt active filter cannot compensate voltage harmonics of the load. Figure 2.19(c) shows that the shunt active filter can compensate current harmonic of the load and voltage harmonic of the source. In Figure 2.19, Z_s and Z_F are impedances of the source and shunt passive filter, respectively. I_{Lh} , V_{Lh} , and V_{sh} are the current harmonic of the load and voltage harmonic of the load and source, respectively. I_{AF} is the current of the shunt active filter. For canceling the harmonic at the point of common coupling (PCC) in Figure 2.19(a), we must have:

$$I_{AF} = I_{Lh} \quad (2.14)$$

In Figure 2.19(b), it is clear that the shunt active filter cannot compensate the load voltage harmonics. In Figure 2.19(c), for canceling load current harmonic and source voltage harmonic, we must have:

$$I_{AF} = I_{Lh} - \frac{V_{sh}}{Z_F} \quad (2.15)$$

Figure 2.20 shows a single-phase voltage source shunt active filter. Shunt active filters are used to compensate current harmonics of nonlinear loads to perform reactive power compensation and to balance inbalance currents. A shunt active filter senses the load current and injects a current into the system to compensate current harmonics or reactive load. These shunt active filters are commercially available on the market.

Marks and Green [36] compared the rating of series and shunt active filters. In their study a shunt filter was used to compensate the current harmonics of

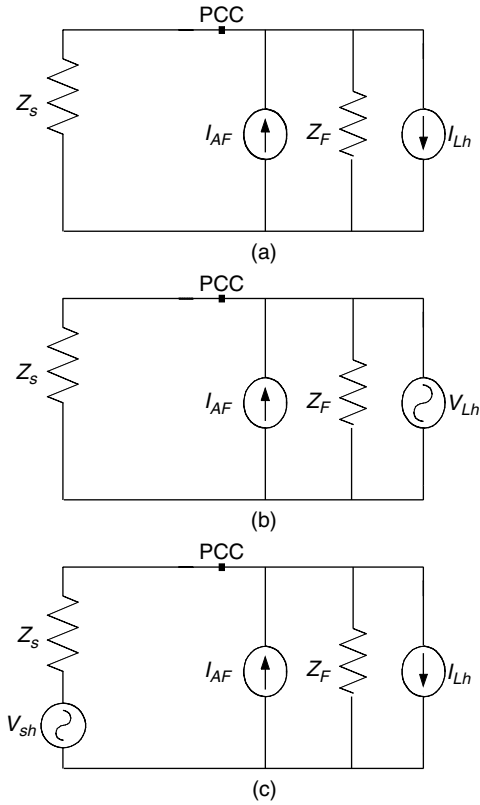


FIGURE 2.19 Equivalent circuit of shunt active filter, source, and load, (a) compensating current harmonic of the load, (b) compensating voltage harmonic of the load, and (c) compensating voltage harmonic of the source.

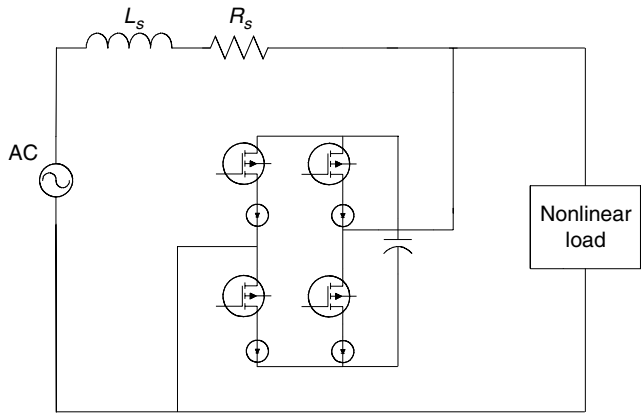


FIGURE 2.20 A typical single-phase voltage source shunt active filter.

a six-pulse distorting current-type rectifier, and a series filter was employed to compensate voltage harmonics of a six-pulse distorting voltage-type rectifier. This means that these active filters cannot do each other's job. They found that the shunt filter has approximately half of the switch power rating of the series filter. The peak voltage over the switches in the series filter is about one-third of the peak voltage over the switches in the shunt filter.

The shunt active filter acts as a current source. The sum of its current and load current is the total current that flows through the source. Therefore, controlling the output current of the active filter can control the source current. Figure 2.21 shows the currents of source, load, and active filter of Figure 2.20 when the shunt filter acts as a harmonic suppressor.

2.5.4 Series Active Filters

Series active filters can be single-phase or three-phase and use voltage or current source inverters. Figure 2.22 shows the equivalent circuit of a series active filter, source, and load when the series filter is used to compensate the current and voltage harmonics. In Figure 2.22(a), the active filter compensates the harmonic current of the nonlinear load, which produces harmonic currents. In Figure 2.22(b), the series active filter compensates voltage harmonics of the load. In Figure 2.22(c), it is shown that the series filter can compensate the current harmonics of the load and the voltage harmonics of the source. For canceling the harmonics at PCC in Figure 2.22(a), we must have

$$V_{AF} = Z_F I_{Lh} \quad (2.16)$$

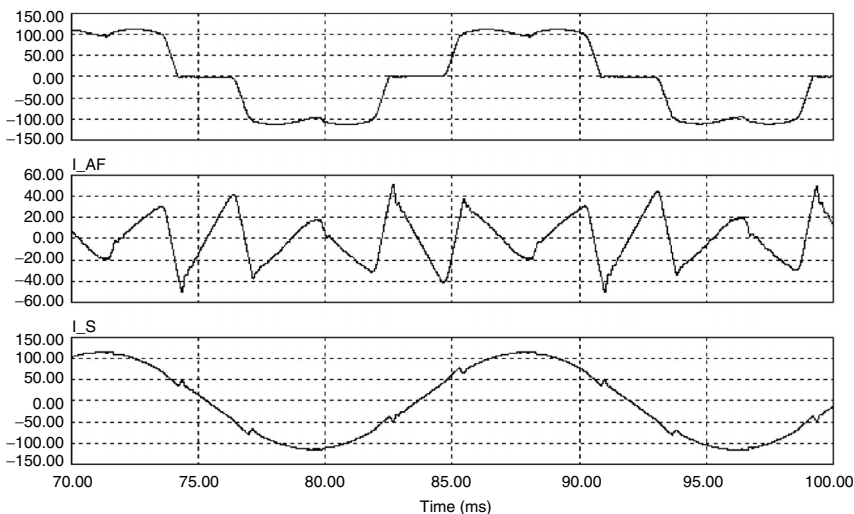
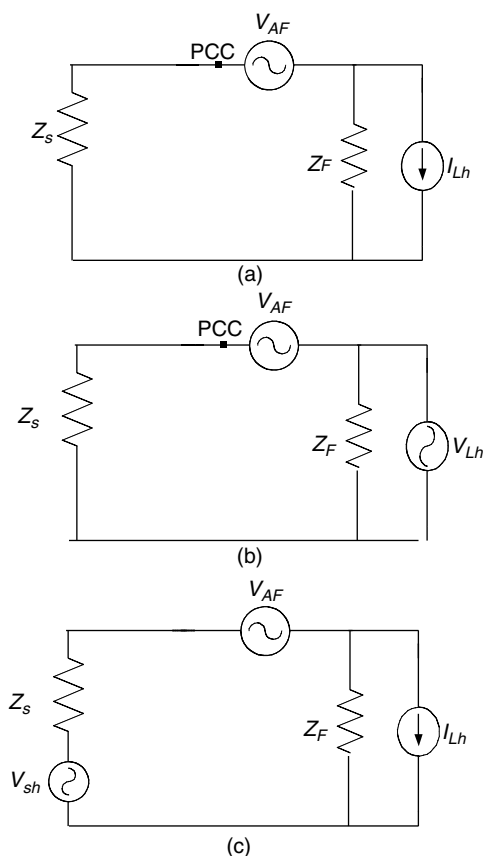


FIGURE 2.21

Current of load, active filter, and source in the system of Figure 2.20.

**FIGURE 2.22**

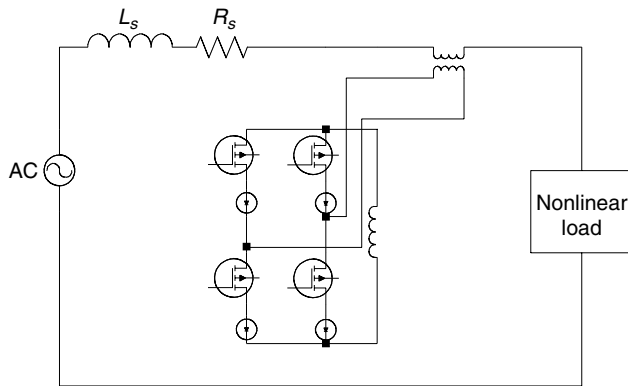
Equivalent circuit of a series active filter, source, and load, (a) compensation of current harmonics of load, (b) compensation of voltage harmonics of load, and (c) compensation of voltage harmonics of source and current harmonics of load.

In Figure 2.22(b), it is clear that, when $V_{AF} = V_{Lh}$, voltage harmonics of load will be cancelled. In Figure 2.22(c), for canceling load current harmonics and source voltage harmonics, we must have

$$V_{AF} = V_{sh} + Z_F I_{Lh} \quad (2.17)$$

Figure 2.23 shows a single-phase, current source series active filter. A series active filter is mostly used to compensate voltage harmonics produced by nonlinear loads as well as voltage regulation and voltage imbalance compensation.

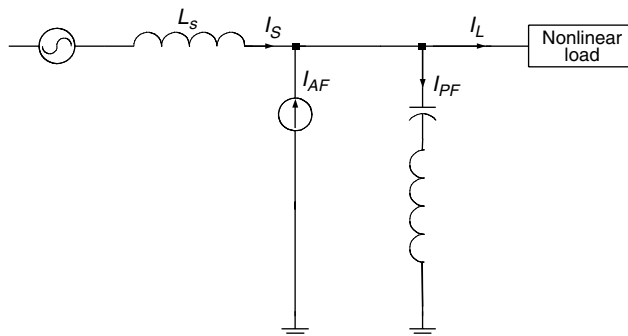
Series active filters are located in series between source and nonlinear loads. In the presence of source side impedance, voltage harmonics of the nonlinear load appear on the point of common coupling. The series active filter senses the load side voltage and produces the harmonic of the load voltage in the negative direction and makes the voltage of the point of common coupling free of harmonics [37].

**FIGURE 2.23**

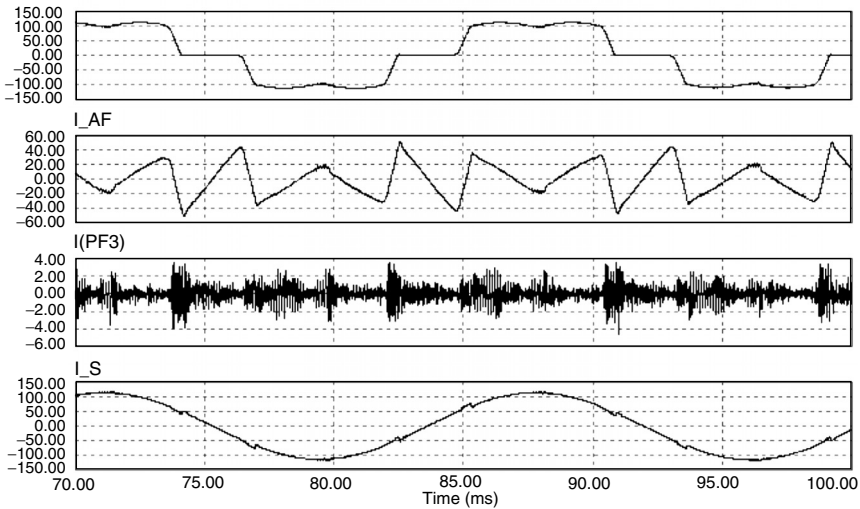
A typical single-phase current source series active filter.

2.5.5 Hybrid Active Filters

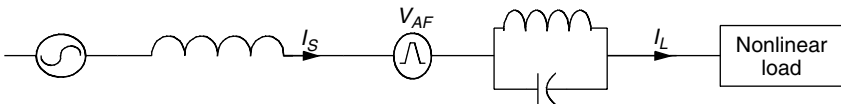
The main purpose of using a hybrid of active and passive filters is to reduce the initial cost of the filter and improve the efficiency. Many configurations of combinations of active filters and passive filters have been studied and developed. Experimental results of the combination of series and shunt active filters with shunt passive filters are presented by Akagi [38] and Peng [39]. Usually, the passive filter is tuned up at a specific frequency to suppress that frequency and decrease the power rating of the active filter. Shunt passive filters should also be of the high-pass type to cancel the switching frequency of the active filter and high-frequency harmonics. In this case, the switching frequency of the active filter will decrease. Figure 2.24 shows a hybrid filter of shunt active and shunt passive filters. The shunt active filter is shown as a current source. Figure 2.25 shows the currents of the passive filter, active filter, load, and source of Figure 2.24. Figure 2.26 shows a combination of a series active filter and a series passive filter.

**FIGURE 2.24**

Hybridization of active and passive shunt filters.

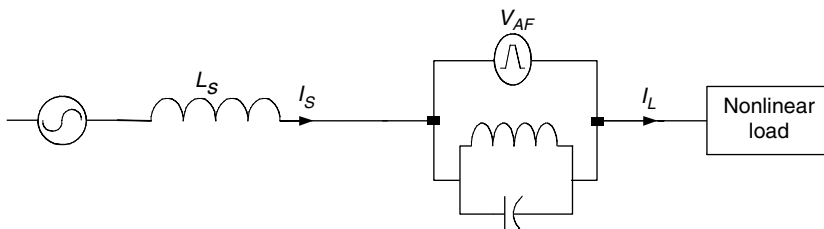
**FIGURE 2.25**

Typical current waveforms of active filter, passive filter, source, and load.

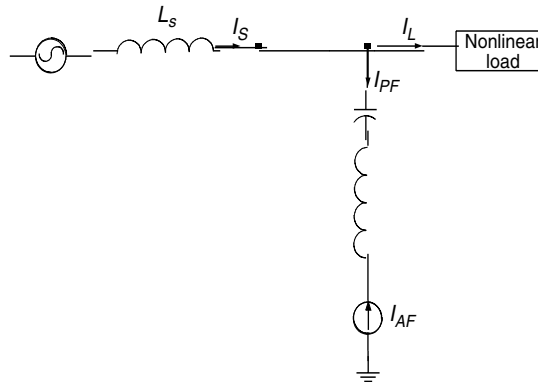
**FIGURE 2.26**

A typical combination of a series active filter and a series passive filter.

Another problem with active filters is the high fundamental current through the series active filter and the high fundamental voltage across the shunt active filter. Paralleling of a series active filter with a passive filter can solve the high current problem in the series configuration. Figure 2.27 shows this combination. A proper control strategy should be adopted to avoid the possibility of resonance. The high voltage across the shunt active filter is

**FIGURE 2.27**

Combination of a series active filter and passive filter for decreasing the high current through the active filter.

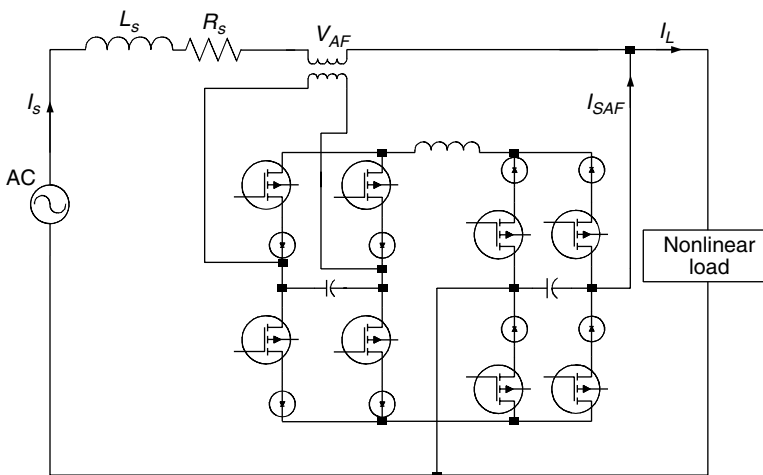
**FIGURE 2.28**

Combination of shunt active filter and passive filter for decreasing the high voltage across the active filter.

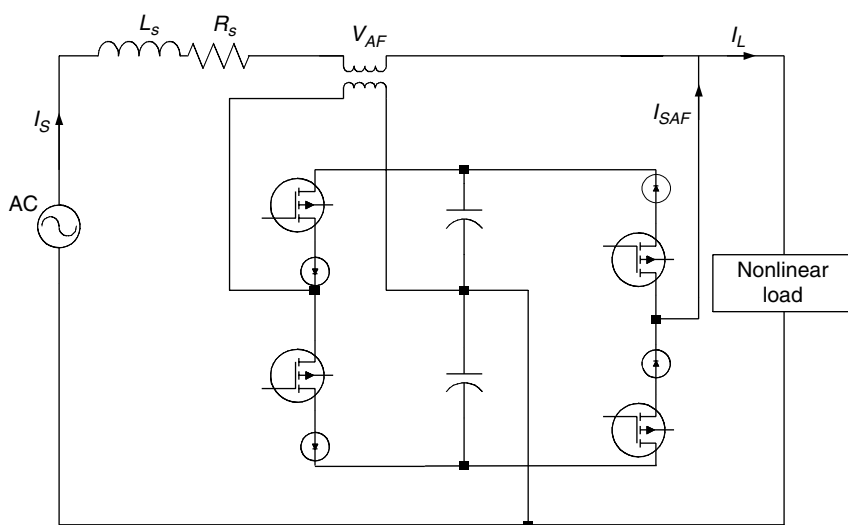
reduced by placing the shunt active filter in series with a passive filter. This kind of configuration is shown in Figure 2.28.

2.5.6 Unified Power Quality Conditioners

UPQCs, also known as universal active filters, are effective devices to improve power quality [40]. A combination of series and shunt active filters forms UPQC. Series active filters suppress and isolate voltage harmonics and shunt active filters cancel current harmonics. Usually, the energy storage device is shared between the two filters either in current source or voltage source configuration. Figure 2.29 shows a single-phase

**FIGURE 2.29**

A typical single-phase current source UPQC.

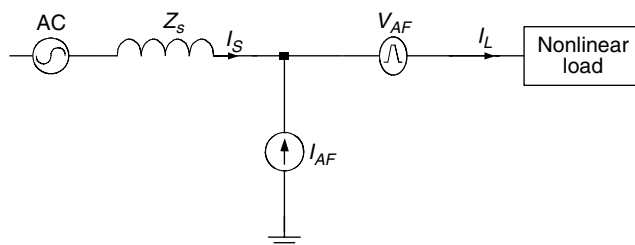
**FIGURE 2.30**

A typical single-phase reduced-parts voltage source-type UPQC.

current source UPQC. Figure 2.30 shows a single-phase reduced-parts voltage source-type UPQC. The number of switches in this reduced-parts UPQC is decreased to four.

There are two kinds of UPQC. In the first type, a shunt active filter is placed near the source and a series active filter is placed near the load as shown in Figure 2.31. The series active filter is used to compensate the voltage harmonics of the load, and the shunt active filter is used to compensate the residual current harmonics and improve the power factor or balance the imbalance load.

In the second type, shown in Figure 2.32, a shunt active filter is placed near the load to compensate the current harmonics of the load. A series active filter is placed near the source to compensate voltage harmonics of the source or regulate the voltage.

**FIGURE 2.31**

First type of UPQC.

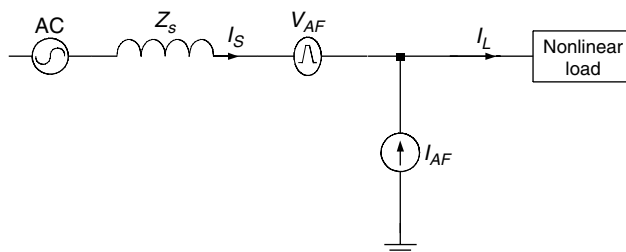


FIGURE 2.32
Second type of UPQC.

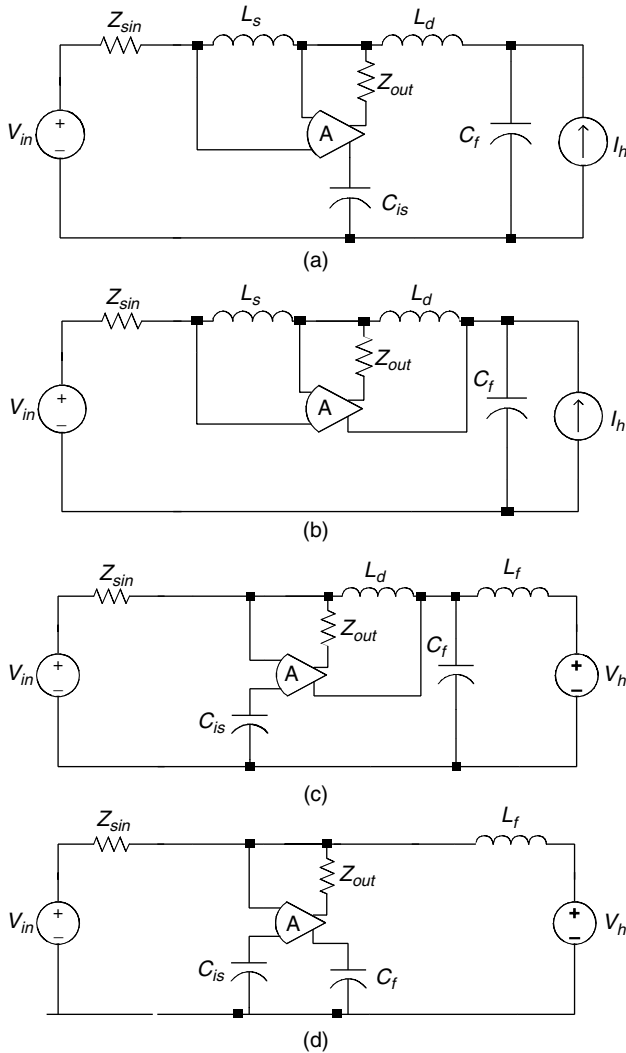
2.6 Active Filters for DC/DC Converters

Active filters for DC/DC converters are divided into two main groups based on the applications. Active filters in the first group are designed to decrease the electromagnetic interference (EMI). The first EMI active filter was introduced by Walker [41] and developed by LaWhite [42]. This type of active filter is mainly used to reduce the radio frequency (RF) emissions of the input current of the DC/DC converters. Theoretically, they were introduced for voltage emission mitigation; however, comprehensive experimental or practical verification has not yet been carried out. Active filters in the second group are designed to suppress the high-frequency current or voltage ripples in DC/DC converters. This type of active filter is mostly used to mitigate the current and voltage ripples of the output side of the converters. Great reduction in the size and cost of passive components is achieved by using the active ripple filters.

2.6.1 Active EMI Filters

Mitigation of high-frequency current and voltage ripples is needed in medium or large switching power systems. For attenuation of large ripples, elements of the required passive filter are significant in size, weight, and cost. Additionally, the performance of low-order passive filters is not satisfactory and higher-order passive filters are needed, which may increase the cost and size of the filter. On the other hand, the performance and controllability of a closed loop system decrease in the presence of high-order passive filters. These problems justify the use of the active EMI filters. There is one energy difference between the passive and active filtering. Passive filters absorb the energy of ripples and trade it with the system; but active filters dissipate the energy of the ripples. Hence, active filters must be used for filtering high-frequency and low-energy ripples.

Figure 2.33 shows four possible topologies for these active filters [43]. Figure 2.33(a) and (b) represents current active filters. In Figure 2.33(a), I_h

**FIGURE 2.33**

Four possible topologies for the active EMI filters.

models the high-frequency ripple of the input current of the converter. L_s senses high-frequency currents, and a magnified value of this current is drawn from the line current by the amplifier. The active filter, in fact, represents an inductor, which is of the magnification of $L_d + L_s$ by the amplifier. This inductor shapes a second-order filter with C_f . Capacitor C_b is used to remove the DC voltage of the system from the active filter. L_s , L_d , C_b , and C_f shape a fourth-order passive filter with a magnified capacitor.

The active EMI filters shown in Figure 2.33(a) and (b) compensate the ripple currents by controlling voltage across the inductor L_d . Figure 2.33(c) and

(d) represents active filters for attenuation of the voltage ripple. Three important issues with respect to active filters must be addressed. The first one is the steady-state impedance of the active filters in the current pass of the converter. The second issue is the transient response and performance. The third issue is the power dissipation in the active filters. These three issues and steady-state characteristics of these active filters such as input and output impedance, resonance frequency, and gain of the amplifier are discussed by LaWhite and Schlecht [44].

2.6.2 Active Ripple Filters

In DC/DC converters, there is a high-frequency ripple voltage at the converter output. This ripple is larger in high-current, low-output voltage converters. In modern DC/DC converters, which need smooth and ripple free outputs, this problem should be solved properly. Traditionally, LC passive filters have been used to compensate this ripple. For proper mitigation, this passive filter must have a wide frequency band. This characteristic increases the size and, consequently, the weight and cost of the passive filters. As mentioned for the EMI filters, second-order passive filters cannot mitigate ripples properly. With increasing size and attenuation of the passive filter, the chance of an interaction between the control system and filter increases. On the other hand, changes in the parameters of the passive filters with time and environmental conditions decrease their attenuation [45].

Another passive method for decreasing current ripple in DC/DC converters is the use of coupled inductors. Using coupled inductors, the voltage over output inductor of the converter can be forced to zero and, consequently, the ripple of the current will be zero. Major savings in size, weight, and cost can be achieved using this method. Unfortunately, this method is not applicable to all types of DC/DC converters. Additionally, changes in converter parameters with time and temperature do not allow proper cancellation of the ripple current.

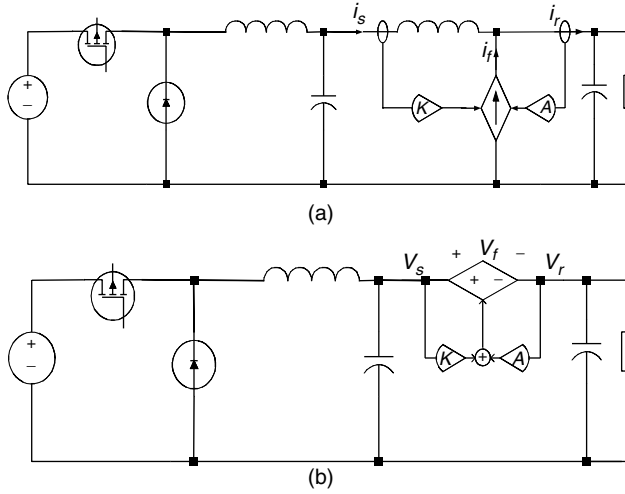
In the same manner as in EMI cancellation, active ripple filters with robust characteristics and better attenuation can provide an alternative for passive filters.

2.6.2.1 Configurations

Two possible configurations for active ripple filters are shown in [Figure 2.34](#). [Figure 2.34\(a\)](#) shows a current ripple active filter [46, 47]. For better performance, the active filter is composed of both feedforward and feedback controllers. The converter is a buck converter, which is convenient for high-current applications.

In [Figure 2.34\(a\)](#), we have

$$i_s + i_f = i_r \quad (2.18)$$

**FIGURE 2.34**

Two possible topologies of the ripple active filters.

where i_s is the ripple current of the sending end and i_r is the ripple current of the receiving end. i_f is the current of the active filter. Since the active filter is composed of two feedforward and feedback controllers, we have

$$i_f = Ki_s + Ai_r \quad (2.19)$$

where K is the gain of the feedforward amplifier and A is the gain of the feedback amplifier. Substituting Equation 2.18 into Equation 2.19, we have

$$i_r = \frac{i_s(1+K)}{(1-A)} \quad (2.20)$$

Since we want to have $i_r = 0$, the magnitude of K must be one with a zero phase shift. The feedback amplifier must have a high gain. Ideally, a feedforward amplifier injects a current in the same manner as the current ripple does in the reverse direction and, therefore, the output ripple will be set to zero. However, because of the nonideality and constraints on sensors and amplifiers, the feedback controller is used to cancel the residual ripple.

Figure 2.34(b) shows a voltage ripple active filter [48]. Similar to the current active filter, both feedforward and feedback controllers are used. This configuration is a dual of the circuit shown in Figure 2.34(a). We have the same equation for this configuration:

$$V_r = \frac{V_s(1+K)}{1-A} \quad (2.21)$$

where V_r is the voltage of the receiving end and V_s is the voltage of the sending end. K and A should have the same characteristics as in Figure 2.34(a).

Current sensors in Figure 2.34(a) must have a high sensitivity, wide frequency range, and zero phase shift. The ideal sensor for this purpose is a well-designed current transformer. The proposed current transformer should have very high magnetizing inductance, small leakage capacitance, and linear characteristics over a wide frequency range.

Voltage sensing in Figure 2.34(b) is simpler than the current sensing. A high-pass active filter can sense the voltage. Phase shift of the high-pass filter should be set as close as possible to zero.

As the power of the ripple current is not too much, a MOSFET- or BJT-based circuit can be used as the current injector. This type of current injector dissipates the energy of the ripple current as shown in Figure 2.35. The use of an LM-type operational amplifier allows a wide band frequency range as large as 10 MHz [49].

The voltage injector in Figure 2.34(b) has more constraints than the current injector. The proposed voltage injector should carry the DC current of the converter. Additionally, it should have a wide frequency range. On the other hand, the voltage injector must isolate the control section from the power section. With these features, a high-frequency voltage transformer with a small magnetizing inductance is a good choice. Figure 2.36 shows a desired current injector. DC current of the converter passes through the very small magnetizing inductor of the transformer. Ripple voltage is induced from the primary side by the control circuit. A complete stability investigation should be carried out to achieve proper compensation.

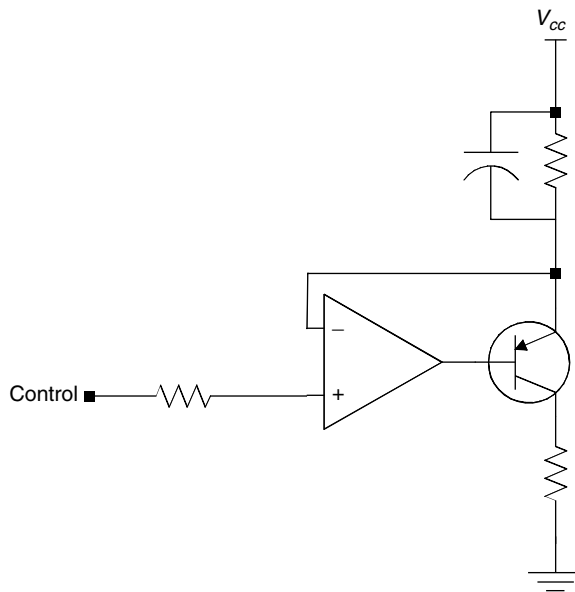
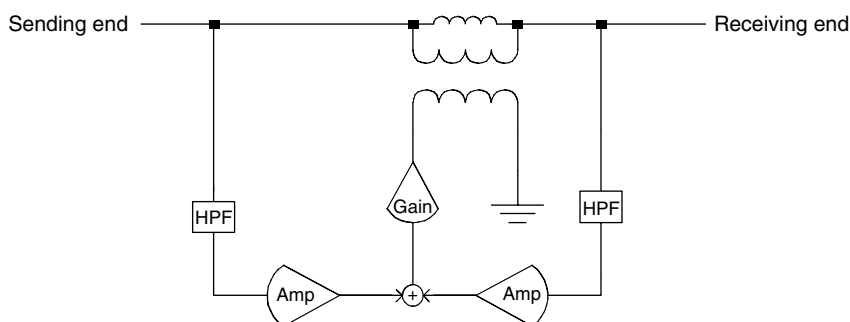


FIGURE 2.35

A simple type of a current injector.

**FIGURE 2.36**

A simple type of a voltage injector.

2.7 Modeling and Analysis

Very few studies have been done on modeling and analysis of active filters. In fact, most of the research has been on modeling of the control system and operating principles of active filters. In this section, we present three modeling methods for modeling of active filters. None of these following three models have been thoroughly studied for active filters.

2.7.1 Switching Function Model

In this model, a switching function must be defined for each switch. The relationship between the input (independent) and output (dependent) parameters of the circuit such as input and output currents and voltages should be expressed via switching functions. For defining the switching functions, control strategy and independent parameters must be determined clearly. All switches in the system are replaced with the switching functions and, therefore, the system is modeled based on the functions. Ordinary analysis is based on the topology. Simulating software packages such as PSpice, PSIM, and Saber[®], which use actual models of the switches, have some problems. The main problems are large produced files, long execution time, and, particularly, convergence problems. There are more problems with other types of software packages like MATLAB[®]/Simulink[®], which uses transfer functions for simulation. For this type of simulation device, all transfer functions for the system must be calculated. Calculation should be revised after each small change in the system. This is cumbersome and sometimes impossible. By using switching functions [50]:

- No actual switch or approximation is needed.
- Most of the system equations are linear.
- A very good and fast system approximation can be achieved.
- It is applicable for every switching scheme.
- The convergence and long execution time are avoided.

An example in this area is presented by Lee and Ehsani [51] for three-phase voltage inverters. This method has not been applied to active filters.

2.7.2 DC Model

A simple DC model can be derived for the analysis and simulation of a system, including source, active filter, and nonlinear load. If we suppose that the three-phase source voltages are balanced, source currents are continuous, and proportion of harmonics to main voltage and current is not large, we can achieve such a model. Figure 2.37 shows a 12-pulse rectifier load and a three-phase shunt active filter. Since the source voltages are balanced, we can use α - β and then d - q transformation to convert the AC parameters of the source into DC values. The relation between the currents of active filters can be expressed as follows:

$$I_{af}(s) = K\tilde{I}_{as}(s) + A\tilde{I}_{al}(s) \quad (2.22)$$

where $\tilde{I}_{as}$ and $\tilde{I}_{al}$ are ripples of the source and load currents.

$$\tilde{I}_{as}(s) = F(s)I_{as}(s) \quad (2.23)$$

$$\tilde{I}_{al}(s) = F(s)I_{al}(s) \quad (2.24)$$

and

$$F(s) = 1 - \frac{\omega_{cut}}{s + \omega_{cut}} \quad (2.25)$$

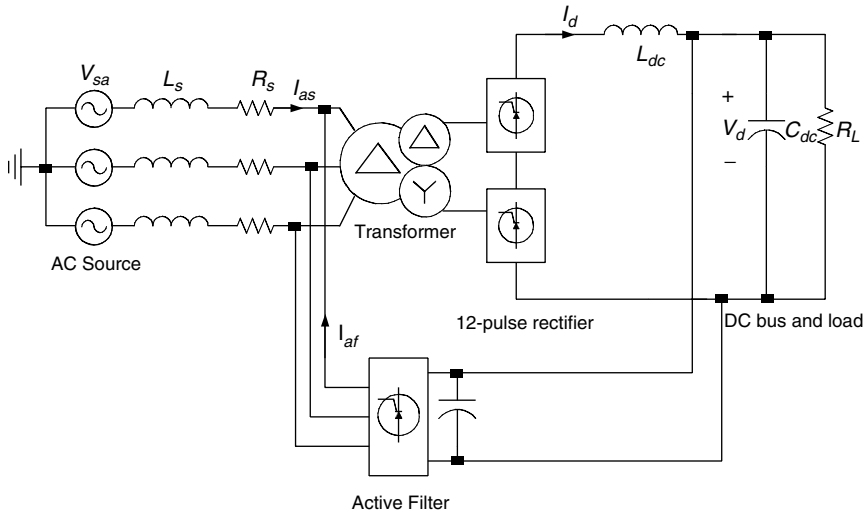
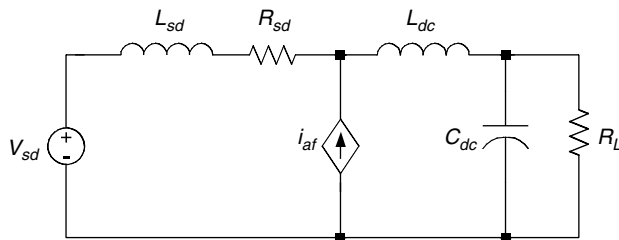


FIGURE 2.37

A three-phase shunt active filter with a 12-pulse rectifier as the nonlinear load.

**FIGURE 2.38**

DC model of the system of Figure 2.37.

where ω_{cut} is the cut-off frequency of the passive filter in the control system of the active filter, which separates ripples of the source and load currents from the fundamental frequency.

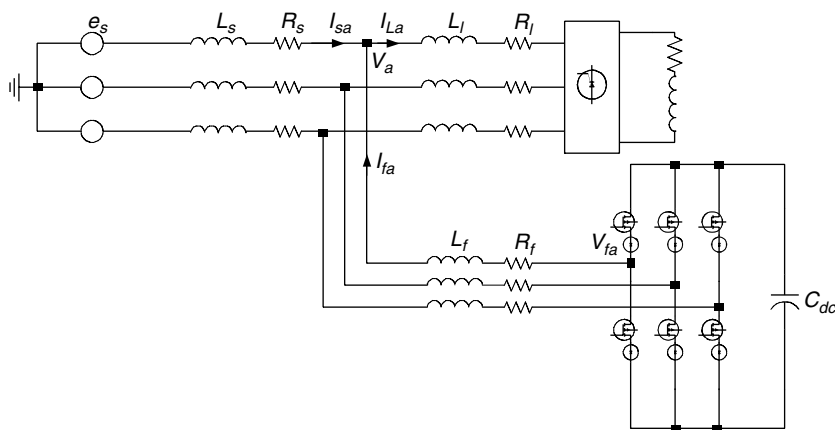
After the above transformation, the whole system is simplified, as shown in Figure 2.38. Transient analysis of the system with high accuracy can be done by the DC model of the system. Srianthumrong and Akagi [52], discuss and analyze a series active filter with a 12-pulse constant voltage load.

2.7.3 Analytical Model

2.7.3.1 Basic Equations

Figure 2.39 shows a three-phase shunt active filter compensating current harmonics of a nonlinear load. The source voltage of the system is a balanced three-phase system. The basic equations of the active filter and the system are as follows:

$$V_{fa} + R_f i_{fa} + L_f \frac{di_{fa}}{dt} = V_a \quad (2.26)$$

**FIGURE 2.39**

A three-phase shunt active filter.

$$V_{fb} + R_f i_{fb} + L_f \frac{di_{fb}}{dt} = V_b \quad (2.27)$$

$$V_{fc} + R_f i_{fc} + L_f \frac{di_{fc}}{dt} = V_c \quad (2.28)$$

We want to use the synchronous reference frame-based method for controlling the active filter. In this method, first, the load current and source voltage should be converted into the d - q base.

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{Lo} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 2 & 3 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (2.29)$$

$$\begin{bmatrix} e_\alpha \\ e_\beta \\ e_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 2 & 3 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (2.30)$$

d - q current and voltage are:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix}, \quad \begin{bmatrix} e_d \\ e_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \quad (2.31)$$

By substituting Equations 2.29 through 2.31 into Equations 2.26 through 2.28 and considering that the system is a balanced three-phase three-wire system, that is, i_{Lo} and e_o are zero, we have

$$v_{df} = -L_f \frac{di_{df}}{dt} + e_d + \omega L_f i_{qf} \quad (2.32)$$

$$v_{qf} = -L_f \frac{di_{qf}}{dt} + e_q + \omega L_f i_{df} \quad (2.33)$$

and

$$e_d = E_m, e_q = 0 \quad (2.34)$$

i_{Ld} and i_{Lq} in Equation 2.31 consist of a DC and an AC part. The DC part of i_{Ld} produces active power in the load and the AC part of it corresponds to the current harmonics. The DC part of i_{Lq} corresponds to the reactive current and the AC part of it corresponds to the current harmonics. Reference currents

for the active filter in d and q axis are

$$i_{df}^* = -\tilde{i}_{Ld} \text{ and } i_{Lq}^* = -i_{Lq} \quad (2.35)$$

where $\tilde{i}_{Ld}$ denotes the AC value of i_{Ld} .

The output voltage of the active filter v_{df} and v_{qf} can be obtained from Equations 2.10 and 2.11:

$$v_{df}^* = -L_f \frac{di_{df}^*}{dt} + e_d + \omega L_f i_{qf}^* \quad (2.36)$$

$$v_{qf}^* = -L_f \frac{di_{qf}^*}{dt} + \omega L_f i_{df}^* \quad (2.37)$$

and the abc axis voltage of the active filter can be obtained as

$$\begin{bmatrix} v_{\alpha f}^* \\ v_{\beta f}^* \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} v_{df}^* \\ v_{qf}^* \end{bmatrix}, \quad \begin{bmatrix} v_{\alpha f}^* \\ v_{\beta f}^* \\ v_{cf}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{\alpha f}^* \\ v_{\beta f}^* \end{bmatrix} \quad (2.38)$$

Usually, a PI controller is used to control the output voltage of the active filters. The transfer function of the output voltage to the reference voltage is as follows:

$$\frac{V_f}{V^*} = \frac{(1 + K_{Pv})s + K_{Iv}}{K_{Pv}s + K_{Iv}} \quad (2.39)$$

where V_f is the output voltage of the active filter and V^* is the reference voltage.

2.7.3.2 Time Delay for Extraction of Reference Current

As mentioned before, the current of d -axis i_{Ld} consists of two portions, DC part and AC part, which correspond to the fundamental and harmonic currents. For achieving reference current, the AC part must be extracted from i_{Ld} . A high-pass filter can perform this task. Figure 2.40 shows the desired filter. Hence, a time delay does not have any meaning in DC values; there is no time delay for extracting the reference current.

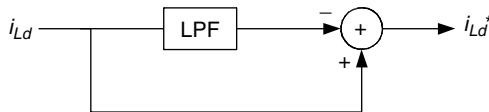
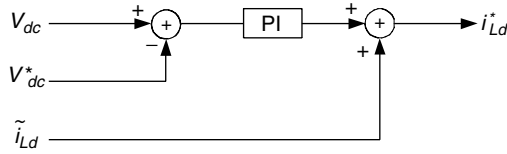


FIGURE 2.40

Desired passive filter for extracting the reference current.

**FIGURE 2.41**

Controller for the voltage of the DC bus.

2.7.3.3 Time Delay of Response for Current

Transfer functions of d - q axis output currents of the active filter over its output voltage cannot be obtained separately for each axis. Transfer functions for I_{df} and I_{qf} can be obtained from Equations 2.36 and 2.37 as follows:

$$\begin{bmatrix} I_{df} \\ I_{qf} \end{bmatrix} = \begin{bmatrix} \frac{-(L_f s + R_f)}{(L_f s + R_f)^2 + \omega^2 L_f^2} & \frac{-\omega L_f}{(L_f s + R_f)^2 + \omega^2 L_f^2} \\ \frac{-\omega L_f}{(L_f s + R_f)^2 + \omega^2 L_f^2} & \frac{-(L_f s + R_f)}{(L_f s + R_f)^2 + \omega^2 L_f^2} \end{bmatrix} \begin{bmatrix} V_{df} \\ V_{qf} \end{bmatrix} + \begin{bmatrix} \frac{-(L_f s + R_f)}{(L_f s + R_f)^2 + \omega^2 L_f^2} \\ \frac{-\omega L_f}{(L_f s + R_f)^2 + \omega^2 L_f^2} \end{bmatrix} E_d \quad (2.40)$$

2.7.3.4 Control of DC Bus Voltage

For controlling the voltage of the DC bus and reducing voltage ripple, a current proportional to the actual voltage and reference voltage should be drawn from the power system. This current must be added to the reference current of the active filter. A simple PI controller can control this current. The transfer function of this PI controller must be considered in the whole system. Figure 2.41 shows this controller.

In the whole model, first, the reference current should be obtained from Equation 2.35 and, after that, the output of the controller of the DC bus voltage must be added to this current. Reference voltage comes from Equations 2.38 and 2.39. Equation 2.40 shows the dynamics of the system [53, 54].

2.8 Control Strategies

Many control techniques have been designed, developed, and realized for active filters. We classify all control methods into two main groups. In the first group, we discuss reference parameter detection methods. This can be done in either the time or frequency domain. In the second group, we discuss derivation methods of the switching functions for active filters.

2.8.1 Reference Current/Voltage Detection Method

This group is divided into time domain and frequency domain analysis.

2.8.1.1 Time Domain Analysis

2.8.1.1.1 High-Pass Filter Method

In this method, a high-pass filter removes the fundamental part of the load current and the remaining part is the harmonic current, which is the reference for the active filter. This method has a high error in the phase and magnitude of the harmonics. Additionally, this method is sensitive to the high-frequency noise.

2.8.1.1.2 Low-Pass Filter Method

A low-pass filter is used in this method to remove the high-frequency components in load current and give the fundamental part. The reference current for the active filter is obtained by subtracting this fundamental part from the load current. Like the previous method, this method has a high error in the phase and magnitude.

2.8.1.1.3 Instantaneous Reactive Power Algorithm

This method, which is also named the $p-q$ method, was introduced for active filter applications by Akagi in 1984 [55]. In this method, the current and voltage of the system are converted into the $\alpha-\beta$ system using the following equations:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 2 & 3 \\ 0 & \sqrt{3} & -\sqrt{3} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.41)$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 2 & 3 \\ 0 & \sqrt{3} & -\sqrt{3} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (2.42)$$

Based on the $p-q$ theory, we have

$$p = v_o i_o + v_a i_a + v_b i_b \quad (2.43)$$

$$q = v_a i_a - v_b i_b \quad (2.44)$$

When the system is a symmetric three-phase or there is no neutral point, we have

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (2.45)$$

The active and reactive power in Equation 2.45 can be decomposed into two AC and DC parts. The DC part resulted from the fundamental current and voltage and the AC part resulted from the harmonics.

$$\begin{aligned} p &= \bar{p} + \tilde{p} \\ q &= \bar{q} + \tilde{q} \end{aligned} \quad (2.46)$$

If just harmonic cancellation is considered, reference currents should be determined based on the DC values of p and q . If reactive current compensation is also considered, the reference current should be determined based on the DC value active power. In the latter case, we have

$$\begin{bmatrix} i_{\alpha}^* \\ i_{\beta}^* \end{bmatrix} = \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} v_{\alpha} & -v_{\beta} \\ v_{\beta} & v_{\alpha} \end{bmatrix} \begin{bmatrix} \bar{p} \\ 0 \end{bmatrix} \quad (2.47)$$

where * denotes the reference value. These are reference values for the source currents. Therefore, the reference value for the active filter is as follows:

$$\begin{aligned} i_{\alpha AF}^* &= i_{\alpha}^* - i_{La} \\ i_{\beta AF}^* &= i_{\beta}^* - i_{L\beta} \end{aligned} \quad (2.48)$$

and the abc reference values for the active filter is

$$\begin{bmatrix} i_{aAF}^* \\ i_{bAF}^* \\ i_{cAF}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{\sqrt{2}} & \frac{\sqrt{3}}{2} \\ -\frac{1}{\sqrt{2}} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{\alpha AF}^* \\ i_{\beta AF}^* \end{bmatrix} \quad (2.49)$$

Figure 2.42 shows the block diagram of this method. For compensation of reactive power and harmonic currents, the dashed part should not be considered. If only harmonic compensation is requested, the dashed part should be added to the diagram.

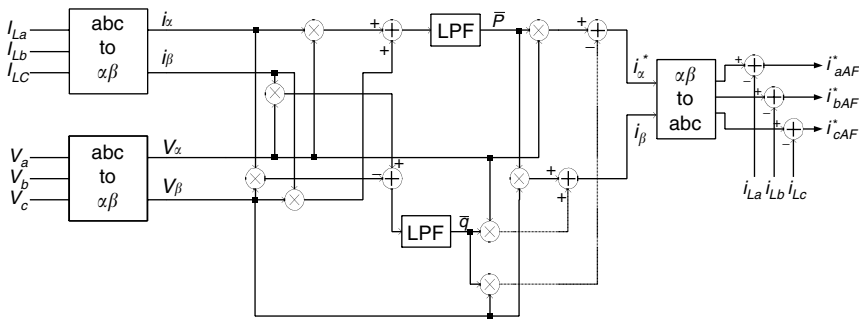


FIGURE 2.42

Block diagram of the instantaneous reactive power algorithm.

This method works properly when the three-phase system is balanced and also when three-phase voltages are pure and harmonic free. Otherwise, the result is poor [56].

2.8.1.1.4 Modified Instantaneous Reactive Power Algorithm

In the modified p - q method [57], p and q are defined as

$$\begin{aligned} p &= v_a i_a + v_b i_b + v_c i_c \\ q &= v'_a i_a + v'_b i_b + v'_c i_c \end{aligned} \quad (2.50)$$

where v'_a , v'_b , and v'_c are -90° shifted line voltage values. By considering the following equation in a balanced system:

$$i_a + i_b + i_c = 0 \quad (2.51)$$

we have

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_a - v_c & v_b - v_c \\ v'_a - v'_c & v'_b - v'_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \quad (2.52)$$

Again, p and q have AC and DC values, where the DC part resulted from the fundamental current and voltage and the AC part resulted from the harmonics. For obtaining the reference currents for only harmonic cancellation, we have

$$\begin{bmatrix} i_a^* \\ i_b^* \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v'_b - v'_c & v_c - v_b \\ v'_c - v'_a & v_a - v_c \end{bmatrix} \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} \quad (2.53)$$

where $\Delta = (v_a - v_c)(v'_b - v'_c) - (v_b - v_c)(v'_a - v'_c)$ and $i_c^* = -(i_a^* + i_b^*)$.

2.8.1.1.5 Synchronous Reference Frame Method

In this method, we utilize the p - q theory to obtain $i_{L\alpha}$ and $i_{L\beta}$ and, after that, with a transformation, we shift the frequency of $i_{L\alpha}$ and $i_{L\beta}$ 60(50) Hz back. With this transformation, the fundamental component of the current will be DC and all harmonics will remain AC [58].

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \quad (2.54)$$

where $\theta = \omega t$ and ω is the angular frequency. With a simple high-pass filter, the DC part can be easily removed from i_{Ld} and i_{Lq} and the remaining can be transformed into its previous frequency with a reverse transformation. Hence, time and phase delays do not have any meaning in DC; we can obtain the oscillating part of i_{Ld} and i_{Lq} without phase and magnitude errors.

$$\begin{bmatrix} i_{AF\alpha}^* \\ i_{AF\beta}^* \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} \tilde{i}_{Ld} \\ \tilde{i}_{Lq} \end{bmatrix} \quad (2.55)$$

Afterward, with a Park transformation as in the p - q method, reference currents for the active filter are obtained.

$$\begin{bmatrix} i_{aAF}^* \\ i_{bAF}^* \\ i_{cAF}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{\alpha AF}^* \\ i_{\beta AF}^* \end{bmatrix} \quad (2.56)$$

In the synchronous reference frame method, the negative component of the line current will be canceled. If we do not want to cancel the negative component, we must subtract this part from the reference current of the active filter. This method is only suitable for three-phase systems and works fairly under nonsinusoidal conditions. Figure 2.43 shows the block diagram of this method. If compensation of the negative component of current is required, the dashed part of the diagram should not be considered.

2.8.1.1.6 Modified Synchronous Reference Frame Method

In this method, there is no need for phase lock loop (PLL) and synchronization. We can obtain i_{Ld} and i_{Lq} from the following equation:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{4\pi}{3}\right) \\ -\sin \theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{4\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.57)$$

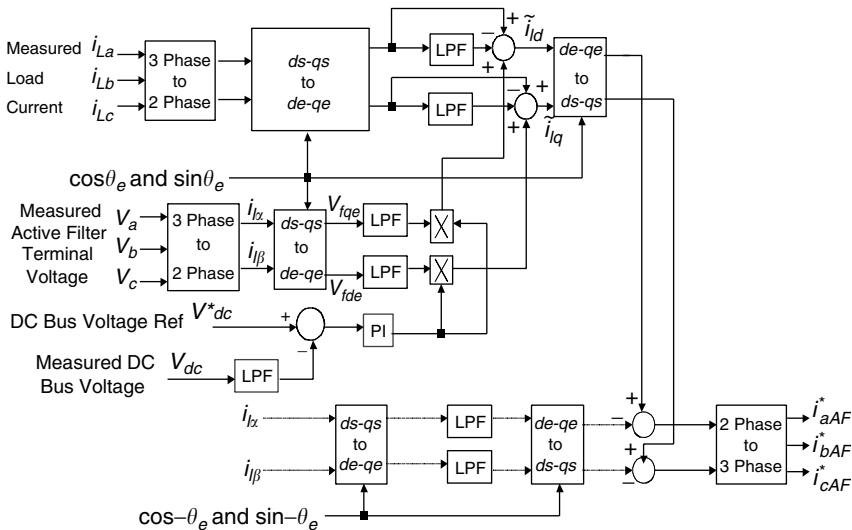


FIGURE 2.43

Block diagram of the synchronous reference frame method.

where $\cos \theta = v_\alpha / (\sqrt{v_\alpha^2 + v_\beta^2})$, $\sin \theta = v_\beta / (\sqrt{v_\alpha^2 + v_\beta^2})$, and v_α and v_β are from the p - q theory. It should be noted that this method is only applicable to the three-phase systems [59].

2.8.1.1.7 Unity Power Factor Method

This method is based on the fact that the source prefers to see a resistive load. We define G as the conductance of the system where:

$G = \langle vi \rangle / \langle v^2 \rangle$, $\langle \rangle$ shows the average value. We have the reference value for the current of the active filter as follows:

$$i_{AF}^* = i_L - Gv \quad (2.58)$$

This method is only suitable for a combination of harmonic and reactive current cancellation [60].

2.8.1.1.8 Sliding Mode Control

In sliding mode control, reference current and voltage must be obtained from one of the above methods. Afterward, a sliding surface is defined as follows:

$$\begin{aligned} i &= i^* \\ s &= i - i^* = 0 \end{aligned} \quad (2.59)$$

The control strategy attempts to place the circuit's parameters in this surface. A control system based on the location of variables relative to the sliding surface gives the suitable commands to the switches. After defining the sliding surface, we must assure that the surface is stable and there is a control law to make $s\dot{s} \leq 0$, where $\dot{s}$ is the differentiation of s . By substituting the equation into the stability equation, a strategy for each switch can be achieved. A PI controller can be used as an outer control loop for controlling the DC voltage [61].

2.8.1.1.9 Passivity-Based Control

In passivity-based analysis, first the differential equations of the active filter and system should be written. Then, functions for switches can be derived directly from the circuit parameters and their derivatives. The stability of the system should be investigated via the system's state equations by the Lyapounov function. The problem associated with this method is that all of the currents and voltages in the system should be measured and derivation of the currents should be calculated. References claim that the stability of this system is better than other methods [62, 63].

2.8.1.1.10 PI Controller

PI controller is usually used for controlling the DC energy storage component. Since the active filter does not deliver active power to the system, the

energy of the DC energy storage (capacitor or inductor) should be constant. In practice, the efficiency of active filters is not 100%, and there are some losses in the switches and the DC side. The voltage of the capacitor or current of the inductor decreases because of these losses. On the other hand, in each period, the DC capacitor (inductor) absorbs or delivers energy to the power system. Therefore, there is voltage (current) ripple over this capacitor (inductor). A control strategy must adjust the voltage (current) of this capacitor (inductor). The proposed control technique does not have to be as fast as the controller of the current. Therefore, a *PI* controller is sufficient. Usually, the difference between practical and reference values of the capacitor voltage (inductor current) is passed through a proper *PI* controller. The result should be multiplied by a coefficient of the line voltage, which is the source of energy. Afterward, the result must be added to the reference current value. In each active filter, we usually have an inner control loop for current control and an outer control loop for DC part control.

2.8.1.1.11 Flux-Based Controller

The idea of the flux-based control method is the same as the synchronous reference frame-based control strategy. After calculation of the current references for the active filter with the synchronous frame, they are converted into fluxes of an active filter output inductor. Fluxes of line voltage and output of the inverter of the active filter are calculated. The switching scheme should regulate the flux of output of the DC/AC inverter to be equal to the sum of the flux of the line and output inductor of the active filter [64].

2.8.1.1.12 Sine Multiplication Method

In this method, the current or voltage of the system is multiplied by a sine wave with the fundamental frequency. The result is integrated over one period; therefore, the harmonic frequency will be removed and only the fundamental frequency will remain, which is the reference for the active filter. The time delay is the problem with this method. As a result, this method is suitable for slow or periodic harmonic systems [65].

2.8.1.2 Frequency Domain Analysis

This method is based on the fast Fourier transformation. The harmonic content of the line voltage or current is obtained by removing the fundamental component by a low-pass filter. Then, the fast Fourier transform of the harmonic is carried out and coefficients for each harmonic are computed. The sampling frequency of the waveform should be greater than twice of the highest frequency to be compensated. Some nonlinear functions should be solved to calculate the switching function for the inverter of the active filter to achieve the same coefficient for the harmonics as calculated before. Numerous modification algorithms have been introduced in different references to improve this method and decrease the computation. The disadvantages of this method are large computation time and time delay. For

calculations of the fast Fourier transform, one whole period of waveform is needed. Some references only calculate the fast Fourier transform for half or quarter of the waveform period. This is valid when the waveform is symmetric over half or quarter of the period [66, 67].

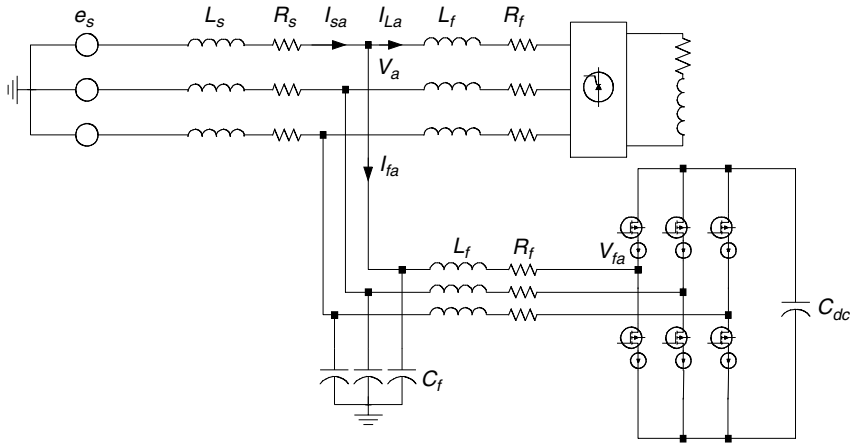
2.8.2 Derivation of Switching Scheme

Several methods have been developed and used for generating switching schemes. The two popular methods are hysteresis and PWM current and voltage controls. Each method has some advantages and disadvantages. The hysteresis method is very fast and very simple to implement. Its switching loss is less than the PWM inverter. In addition, in this method, switching only occurs when the waveform leaves the desired band. The disadvantage of this method is the variable switching frequency. An undesirable white noise is also generated by this variable switching frequency. Furthermore, in the per-phase hysteresis method, phase interaction results in low-frequency error and peak current ripple [68, 69]. PWM current or voltage control methods are well known and can be used with any control method. The PWM method has a very fast response and is very simple to implement. The main disadvantages of this method are high switching losses and high frequency distortion [70]. Other methods that can be used for obtaining switching functions are sliding mode control, deadbeat control, and fuzzy logic control. Sliding mode control was discussed earlier. The main disadvantage of this method is the large amount of calculations. A deadbeat controller has been developed based on the discrete sampling theory and PWM method. A digital signal processor (DSP) must be used to implement this method and the results are good. Theoretically, results that are the same as those of the hysteresis method can be achieved with the constant switching frequency [71].

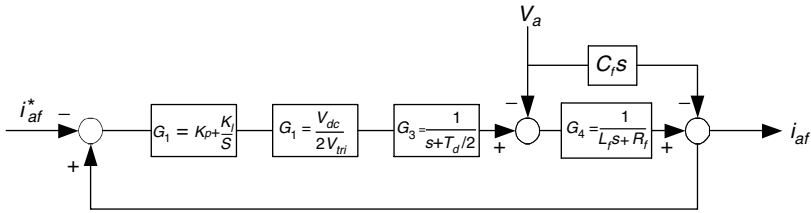
2.9 Stability Assessment

In this section, we discuss the stability of active filters. For stability assessment of active filters, proposed topology should be considered [73–75]. First, we consider a three-phase shunt active filter as the proposed topology. [Figure 2.44](#) shows this active filter beside the AC system, which can be modeled as an AC source, RL series impedance, and a nonlinear load.

There are two main control loops for the active filters [76]: current control loop and voltage control loop. Current control loop is an inner loop for controlling the output current of the active filter and voltage control loop is an outer control loop for controlling the voltage of the DC bus of the active filter. For current control, we use the synchronous reference frame method. A simple PI controller is used for the voltage control loop. For stability assessment,

**FIGURE 2.44**

A three-phase shunt active filter.

**FIGURE 2.45**

Block diagram of the current controller.

the whole system should be modeled to establish a relationship among I_s , I_f , and I_L , which are currents of the source, active filter, and load, respectively [72]. Figure 2.45 shows the block diagram of the current loop control.

G_1 is the transfer function of the PI controller. The time constant of this controller is in the order of the switching frequency, and its minimum gain should be determined from the following equation:

$$\left| \frac{dv_{PWM}}{dt} \right| < \left| \frac{dv_{tri}}{dt} \right| = 4V_{tri}f_{sw} \quad (2.60)$$

Error decreases when the gain increases [74]. G_2 is the gain of the PWM converter and G_3 is the time delay caused by the PWM inverter. T_d is the switching period. For stability study, we can neglect this term. G_4 models the delay of the current of the active filter from the output voltage of the active filter. Maximum of L_f can be determined from the following equation:

$$\left| \frac{di_{Lh}}{dt} \right| < \left| \frac{di_{af}}{dt} \right| = \frac{V_{dc} - \sqrt{3}V_a}{2L_f} \quad (2.61)$$

In our stability studies, we consider harmonic terms of the system and, hence, we are using the synchronous reference frame-based method, which has no delay in generating reference for the active filter; we have

$$i_{af}^* = -i_{Lh} \quad (2.62)$$

where i_{Lh} denotes the harmonic content of the load current. We can consider V_a as a disturbance and the complete transfer function of i_{af} to i_{Lh} will be as follows:

$$G(s) = \frac{V_{dc}(K_p s + K_I)}{2V_{tri}L_f s^2 + (2V_{tri}R_f + V_{dc}K_p)s + K_I} \quad (2.63)$$

This is the transfer function of the open loop system without considering load and power network. Stability assessment of this transfer function with changes in K_p and K_I can be investigated with Bode or Nyquist methods [75]. We consider a power network as a voltage source e_s and a series impedance. L_s , inductance of the source side, is always less than 1 mH [76]. The load is considered as an inductive load. Because the load is a three-phase rectifier, we must consider two states for the load. In the first state, the phase diode is not conducting and, hence, $Y_L = 0$. In the second state, the phase diode is conducting and, therefore, $Y_L = 1/(L_s s + R_L)$. Y_L is the admittance of the load. With these assumptions, the transfer function of the system considering the load and network is presented in Figure 2.46.

The transfer function of the block diagram shown in Figure 2.46 can be written as follows:

$$\frac{I_{af}}{e_s} = \frac{\frac{-G(s)}{1+G(s)} \frac{Y_L}{1+Y_L Z_s} - \frac{Y_{Line}}{1+Y_L Z_s}}{1 - \frac{G(s)}{1+G(s)} \frac{Y_L Z_s}{1+Y_L Z_s} - Y_{Line} \frac{Z_s}{1+Y_L Z_s}} \quad (2.64)$$

$$H(s) = \frac{I_{af}}{e_s} = \frac{-G(s)(Y_L + Y_{Line}) - Y_{Line}}{1 + G(s) + Y_L Z_s - Y_{Line} Z_s - Y_{Line} G(s)} \quad (2.65)$$

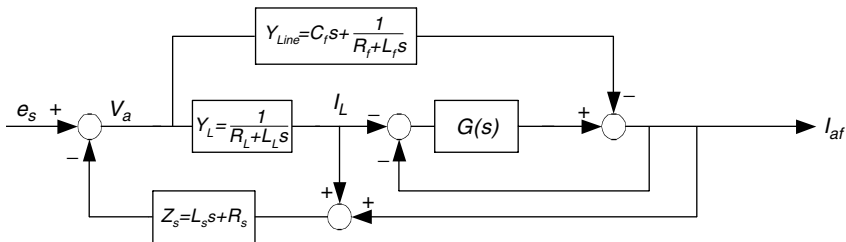
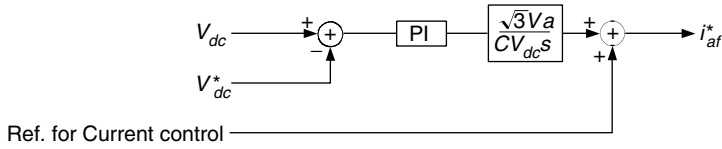


FIGURE 2.46
Block diagram of the whole system with the active filter.

**FIGURE 2.47**

Block diagram of the voltage control.

The stability of the system can be studied by determining poles and zeros of $H(s)$ and phase and gain margins with the Bode plot. Similarly, stability analysis of other topologies such as single-phase shunt active filter and single-phase or three-phase series active filter can be studied.

The outer control loop controls the voltage of the DC capacitor. This voltage changes because of losses in the active filter. Fundamental current should compensate this loss. The real power from the system to the active filter is

$$P_{in} = \sqrt{3} V_a I_1 \quad (2.66)$$

where I_1 is the current with the fundamental frequency. The power loss in the capacitor is equal to [77]:

$$P_c = \frac{dW_c}{dt} = \frac{1}{2} c \frac{dV_{dc}^2}{dt} = c V_{dc} \frac{dV_{dc}}{dt} \quad (2.67)$$

We also obtain:

$$\frac{V_{dc}}{I_1} = \frac{\sqrt{3} V_a}{c V_{dc} s} \quad (2.68)$$

Voltage control block diagram of the DC capacitor is shown in Figure 2.47.

The time constant of this PI controller must be much larger than the time constant of the PI controller for the current control.

2.10 Conclusion

Due to the increase in nonlinear loads in electrical power systems, which produce current and voltage harmonics, the problem of harmonics has become serious, affecting power quality. There are many problems associated with the use of passive filters. Active filters are the emerging devices, which can perform the job of harmonic cancellation properly. In this chapter, harmonics, their causes and effects, and mitigation methods have been discussed. Active filters, their applications, and their different types have also been explained. Furthermore, different control methods, modeling and analysis, and stability assessment for active filters have been described.

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3

Unified Power Quality Conditioners

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Unified power quality conditioners (UPQC), also known as universal active filters, are among the most suitable devices to improve power quality. A combination of series and shunt active filters forms UPQC. The series active filter suppresses and isolates voltage-based distortions such as voltage harmonics, voltage unbalance, voltage flicker, and voltage sag and swell. The shunt active filter cancels current-based distortions such as current harmonics, load unbalance, and neutral current. At the same time, it compensates the reactive current of the load and improves power factor [1].

Usually, the energy storage device is shared between the two active filters. UPQC consists of two bidirectional converters connected to a common DC bus and a series transformer. The series bidirectional converter is rated at a small percent of the nominal power of the load and it is connected via a transformer in series with the AC line. The control function of this converter can be designed to regulate load voltage or to cancel voltage harmonics of the load. The second bidirectional converter is connected in parallel with the load terminals. This converter accomplishes three functions simultaneously. It eliminates the current harmonics of the load. At the same time, it draws reactive current to improve the power factor of the system. A parallel inverter also draws the fundamental current to compensate the power loss of the system, and makes the voltage of DC capacitor constant. UPQC has been shown to be a strong tool to improve power quality in many applications [2, 3].

A new uninterruptible power supply (UPS) topology (series-parallel line-interactive), which is derived from the UPQC topology, has also been attracting the attention of many researchers recently. The main purpose of UPS systems

is to provide critical loads with uninterrupted, reliable, and high-quality power. They need to keep the critical loads running, regardless of the reliability and quality of the main AC power supply. UPS systems, in fact, protect critical loads against power outages as well as over- and under-voltage conditions. UPS applications include medical facilities, life-support systems, data storage and computer systems, emergency equipment, telecommunications, industrial processing, and on-line management systems.

The line-interactive UPS system has better efficiency, but cannot provide tightly regulated output voltage and high input power factor at the same time [4]. The new series-parallel line-interactive UPS topology combines the advantages of both on-line and line-interactive UPS systems. It can simultaneously achieve unity power factor, precise regulation of the output voltage, and high efficiency [5]. Its configuration is shown in Figure 3.1.

A battery pack is considered at the DC bus as the power source. This battery supplies the load, when the input voltage is beyond the specific range or shuts down. When the AC line is within the preset tolerance, most of the power is supplied directly from the AC line to the load. Only a small portion of the total power, usually up to 15%, flows through the series and parallel converters. This power is needed to compensate for any differences between the input and the output voltages and to improve the power factor of the system. At the same time, the parallel inverter draws the fundamental current to charge the battery. On the other hand, when the input voltage shuts down, the static switch separates the source and the load. In this operating mode, the parallel converter acts as a DC/AC inverter and supplies the load from battery pack. Since an important portion of the power flows from the AC line to the load without any conversion, the efficiency is higher than that of an on-line UPS system. Having eliminated the main drawback of double-conversion UPS systems, the series-parallel UPS topology appears to be a strong competitor of on-line UPS systems in many applications [6–9]. In this chapter, we present analysis, control, and steady-state operation of unified

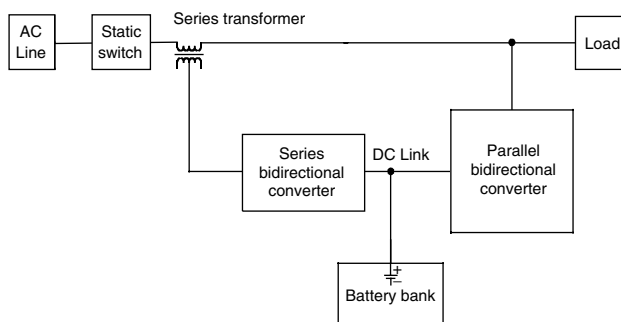


FIGURE 3.1

Block diagram of a typical series-parallel line-interactive UPS.

power quality conditioners (series-parallel active filters) along with series-parallel UPS systems. Topology, current and voltage control, and performance of these systems in different operating modes are explained. Differences and similarities are also described.

3.1 Series-Parallel Configuration

A three-phase unified power quality conditioner consists of two full-bridge bidirectional converters connected to a common DC-link bus. The series bidirectional converter consists of six switches and is rated at a small percent of the nominal power of the load. It is connected via a transformer in series with the AC line. This converter compensates the voltage-based distortions and adjusts the voltage of the load terminal. The parallel converter also consists of six switches and deals with current-based distortions. Two passive filters formed by L_1 , C_1 , L_2 , and C_2 remove switching frequency harmonics from the output current of the parallel converter and the output voltage of the series converter, respectively. L_1 also acts as a link between the filter and the system. Parallel converter delivers its current to the system through this inductor. Its inductance directly influences the bandwidth of the parallel converter. Load is a sensitive nonlinear electronic device. Topologically, the only difference between the series-parallel UPS system (Figure 3.2) and UPQC is the additional battery pack in UPS. In the backup mode of the UPS system, when the input voltage exceeds the defined range, the battery provides power to the load through the parallel converter. In addition, the UPS system must be capable of compensating voltage sag and swell for a long period of time; but in UPQC systems, these distortions are considered short term.

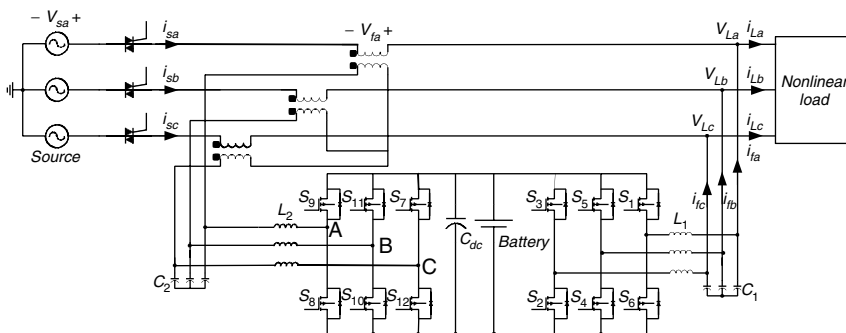


FIGURE 3.2

A series-parallel UPS topology based on two three-leg bidirectional converters.

3.2 Current Control

Basically, current control of the parallel converter in the UPQC system and bypass mode of the UPS system is the same. In both systems, a synchronous reference frame method is used. In the synchronous frame base method, the first three phase instantaneous load currents, i_{La} , i_{Lb} , and i_{Lc} , and source voltages, V_{La} , V_{Lb} , and V_{Lc} are converted into d - q domain.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (3.1)$$

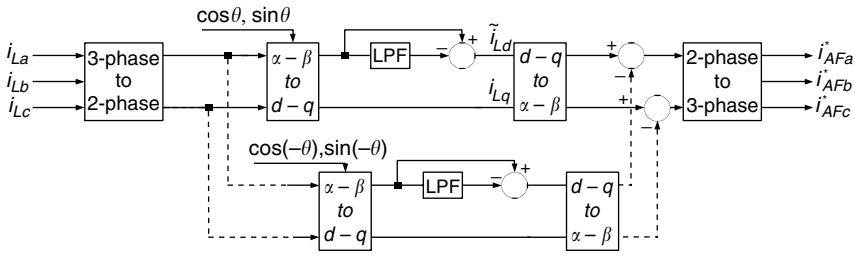
d - q currents and voltages are:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (3.2)$$

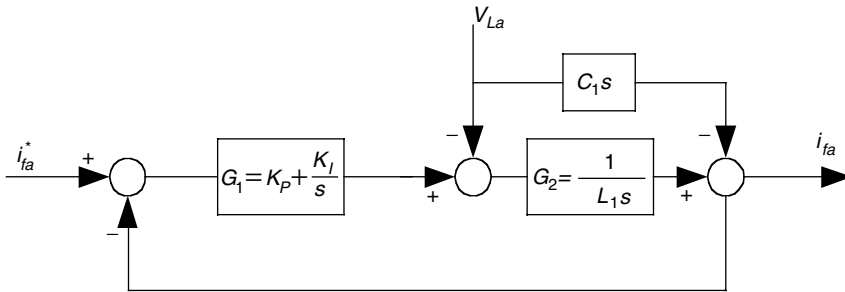
where $\theta = \omega t$ and ω is the angular frequency. v denotes the load current or line voltage. i_{Ld} and i_{Lq} resulting from Equation 3.2 include a DC and an AC part. The DC part of i_{Ld} corresponds to the active power in the load and the AC part of it corresponds to the current harmonics. The DC part of i_{Lq} produces reactive power and the AC part of it produces current harmonics. When harmonic compensation and power factor correction are considered, reference currents for the active filter in d and q axis are:

$$i_{df}^* = -\tilde{i}_{Ld} \quad \text{and} \quad i_{qf}^* = -\tilde{i}_{Lq} - \overline{i_{Lq}} \quad (3.3)$$

where $\tilde{i}_{Ld}$ and $\tilde{i}_{Lq}$ denote AC value of i_{Ld} and i_{Lq} and $\overline{i_{Lq}}$ is the DC value of i_{Lq} . With a simple high-pass filter, the DC part can be easily removed from i_{Ld} and the remaining can be transformed into its previous frequency and three-phase quantity with a reverse transform of Equations 3.2 and 3.1, respectively. Hence, time and phase delay do not have any meaning in DC; we can achieve i_{Lq} and the oscillating part of i_{Ld} without any phase and magnitude error. Figure 3.3 shows the block diagram of the synchronous reference frame method for deriving reference currents for the parallel converter. The dashed part of the block diagram prevents removal of the negative component of the line current. If cancelation of negative component is not suggested, this section must be considered in the block diagram. The three-phase output of this block diagram is used as a reference current for the parallel converter. Figure 3.4


FIGURE 3.3

Block diagram of the synchronous reference method for deriving current references.


FIGURE 3.4

Block diagram of the current control for one phase of the parallel converter.

shows the block diagram of the current controller for each phase. Considering V_L as a disturbance, the transfer function of i_f/i_f^* is

$$\frac{i_f}{i_f^*} = \frac{K_p s + K_I}{L_1 s^2 + K_p s + K_I} \quad (3.4)$$

A typical frequency response of the series converter is shown in Figure 3.5. The bandwidth is mostly affected by L_1 . Bandwidth increases when the inductor decreases. On the other hand, when the inductor decreases, current harmonics with switching frequency appear in the line current. Therefore, an appropriate value must be chosen for this inductor.

A PI controller is used to control the voltage of the DC-link. Fundamental current is needed to recharge the capacitor. The voltage control block diagram of the DC capacitor is shown in Figure 3.6. The low-pass filter cancels any spike or AC disturbance from the DC bus voltage. The time constant of this PI controller must be much larger than the time constant of the PI controller for the current. Multiplying the output of the controller by the DC sequence of $d-q$ component of the line voltage ensures that the fundamental component of the line current is used for charging the battery. Simulation results of current regulation are shown in Figure 3.7.

UPS current control function is the same as the UPQC, except for recharging the battery. In the UPQC system, the fundamental current is a small portion of

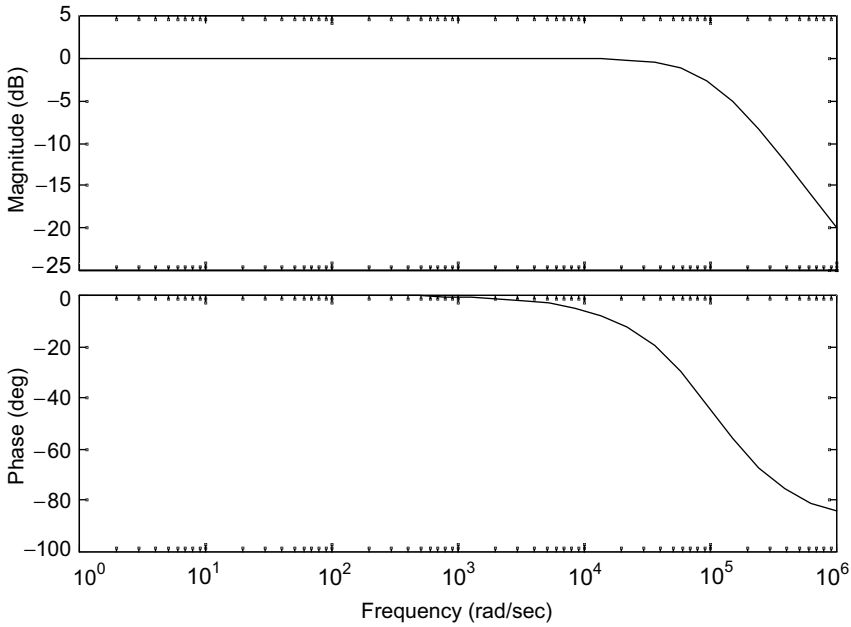


FIGURE 3.5
Typical frequency response of the parallel converter.

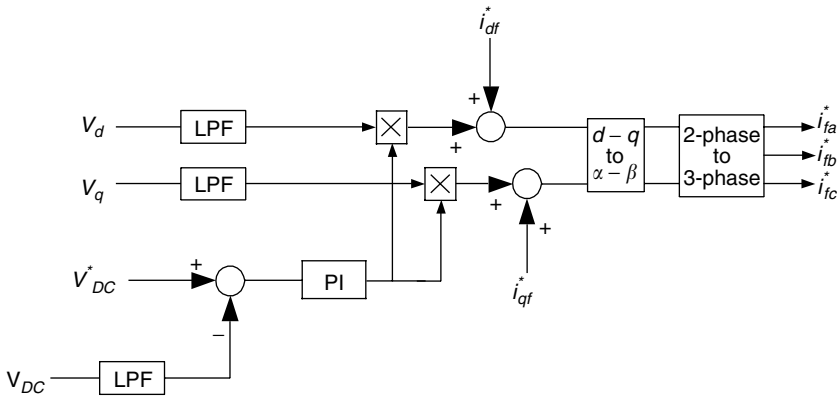
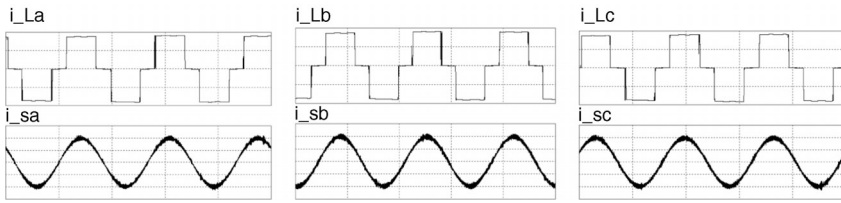


FIGURE 3.6
Block diagram of the DC bus charging.

the current of the parallel converter. Mostly, this current is used to compensate the loss in the system. For charging the battery in the UPS, a continuous fundamental current is needed. For storage systems, the state of charge (SOC) of the battery should be considered. The SOC of the battery can be calculated using voltage, current, and temperature sensors. Usually, the battery of the UPS system consists of 120 lead–acid battery cells with a nominal voltage of 2 V. The

**FIGURE 3.7**

Typical simulation results for the current regulation of each phase by the parallel converter (1 A/div).

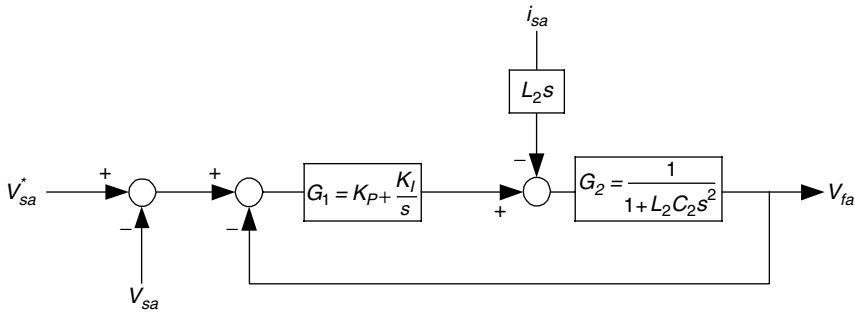
discharge voltage level for this kind of battery is considered to be 1.75 V or 87.5% of the nominal voltage. When the battery is fully charged, there is no need to draw the active current from the source by the parallel converter.

3.3 Voltage Control

In both UPQC and UPS systems, the series converter regulates the line voltage. In the UPQC system, two functions can be defined for this converter. When the load is sensitive and critical, a series converter is used to regulate line voltage for the load. It cancels out any line voltage distortions such as voltage harmonics, sag, swell, and voltage unbalance. It is capable of eliminating any voltage harmonics with a frequency within the bandwidth of the control scheme. After harmonic compensation of the parallel converter, the line current is considered free of harmonics. In this case, for compensating voltage harmonics, there is no need for active power. However, small components of harmonics remain in the line current. Passing through the terminal of the series converter, these current harmonics produce active power. The produced active power charges the DC-link capacitor. For voltage sag (swell) compensation, active power must be delivered to (received from) the system. This active power is supplied (received) by the DC capacitor and creates a voltage ripple on the DC bus voltage.

The second function of the series converter of UPQC, which is mostly considered in very high-power applications, is defined to protect the power system against the voltage distortions originating from the load. Some nonlinear loads, which usually have a capacitor bank after a bridge rectifier, appear to be voltage harmonic generators. The voltage harmonics at the point of common coupling (PCC) affect the other sensitive loads connected to this point. The series converter is capable of suppressing the voltage harmonics of the load.

The voltage of each phase is controlled separately in the system. A three-phase lock loop (PLL) produces the reference voltage for each phase. The inputs of PLL are three-phase voltages of the line and the outputs are three reference voltages for the controller. The block diagram of voltage control for each phase with first functionality of UPQC is shown in [Figure 3.8](#).

**FIGURE 3.8**

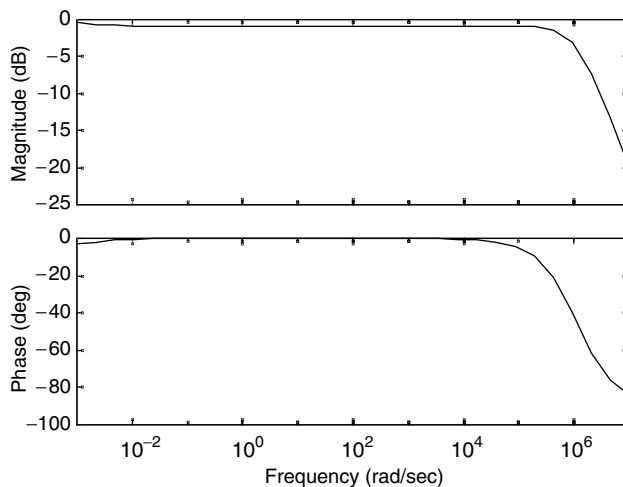
Block diagram of the voltage control for each phase.

Considering i_{sa} as a disturbance, the transfer function of the controller is achieved as

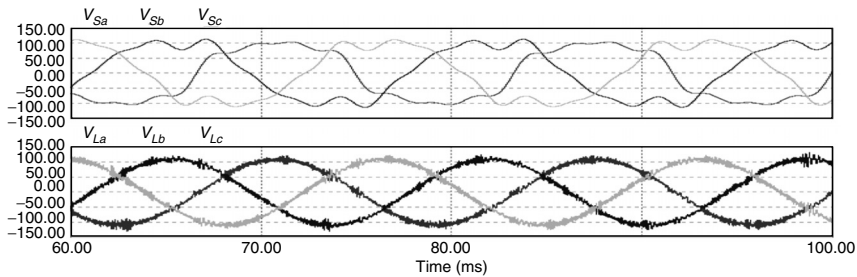
$$\frac{V_{fa}}{V_{sa}^*} = \frac{K_p s + K_I}{L_2 C_2 s^3 + (K_p + 1)s + K_I} \quad (3.5)$$

The frequency response of this transfer is shown in Figure 3.9. The bandwidth of the transfer function is about 20,000 rad/sec. This bandwidth covers most of the voltage disturbances that occur in power systems. Figure 3.10 shows the simulation results of the voltage regulation in the presence of voltage sag and harmonics.

Voltage control of the UPS system is the same as the UPQC system; but load voltage regulation is the only function of the series converter. The presence of the battery allows the compensation of voltage sag/swell for a longer time in an order of hours. Additionally, the stable voltage of the DC bus

**FIGURE 3.9**

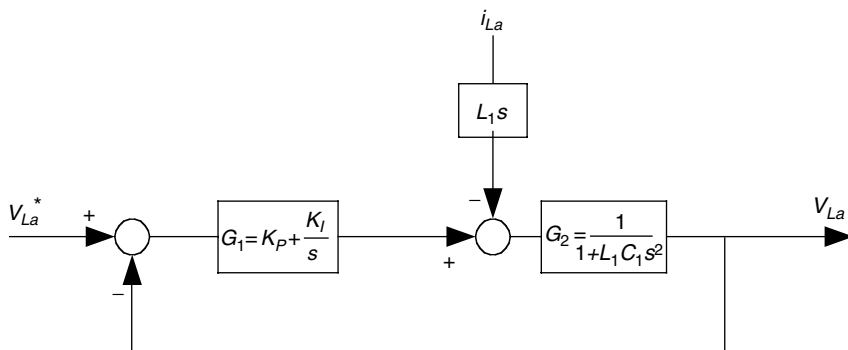
Typical frequency response of the series converter.


FIGURE 3.10

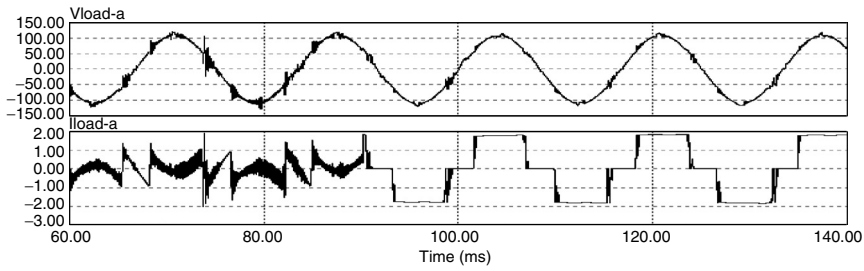
Typical simulation results for the three phases of the series converter in the presence of voltage sag and harmonics.

results in a better cancellation of voltage disturbances. In the UPQC system, taking care of DC bus voltage is one of the permanent functionalities of the controller, which slightly affects the performance of the system. This behavior is evident in simulation and experimental results.

There is an additional operating mode for the UPS system, which does not exist in the UPQC system. When the difference between the input voltage and reference voltage exceeds the specific range, which is determined by the rating of the series converter, the static switch isolates the source, and the parallel converter supplies the load. Under normal conditions, the terminal voltage of the parallel converter, which is the voltage of the load terminal, is regulated by the series converter. After isolation of the source, the parallel converter eliminates all of its controlling functions and supplies the load by a sinusoidal voltage. In fact, there is no hardware transition time from the bypass mode to the backup mode. Therefore, only a limited transition time occurs on the voltage of the load terminal. The reference voltage is the output of the three-phase phase-to-phase PLL, which is freewheeling at 60 Hz. A block diagram of the voltage control of the parallel converter in backup mode is shown in Figure 3.11.


FIGURE 3.11

Block diagram of the voltage control in the backup mode of the parallel converter in a UPS system.

**FIGURE 3.12**

Typical simulation results of transferring from the bypass mode to the backup mode in a UPS system, load voltage (upper waveform), and current of a parallel converter (lower waveform).

When the source voltage recovers, the PLL synchronizes itself with the line voltage. After completion of synchronization, the static switch connects the line, and the series converter starts regulating. Typical simulation results of transferring from bypass to backup mode are shown in Figure 3.12.

3.4 Power Flow and Characteristic Power

In the UPQC and in the bypass mode of UPS system, while the line current is conditioned with the parallel converter, the series converter deals with the input voltage distortions. It injects or receives active power for voltage sag or swell compensation. It also delivers a zero average instantaneous power for voltage harmonic cancelation. The voltage across the series converter is

$$V_f = (V_{ref} - V_s) + \sum V_h = V_s(1 - 1/k) + \sum V_h \quad (3.6)$$

where $k = V_s/V_{ref}$ and V_h is the voltage harmonic of the source. All the voltages are instantaneous values. To indicate the effect of harmonics on the power rating of the converters, we define “characteristic power” instead of the apparent power. This term is defined as

$$CS = I_{rms} V_{rms} \quad (3.7)$$

CS is the characteristic power and I_{rms} and V_{rms} are effective values of current and voltage including harmonics. The value of V_{rms} for the output of the series converter is

$$V_{rms} = (V_1^2 + \sum V_h^2)^{1/2} = V_s [(1/k - 1)^2 + THD_v^2]^{1/2} \quad (3.8)$$

where $V_1 = V_{ref} - V_s$. Considering only active current through the line, the characteristic power of each phase of the series converter is

$$CS_{Series} = V_s I_1 \cos \theta \sqrt{(1/k - 1)^2 + THD_v^2} \quad (3.9)$$

where THD_v is the total harmonic distortion (THD) of the source voltage and is defined as $THD_v = \sqrt{\sum V_h^2} / V_{sr}$, $\cos \theta$ is the power factor of the load, and I_1 is the fundamental component of the load current.

Likewise, while the series converter regulates the voltage of the load terminal, the parallel converter compensates the reactive power of the load and current harmonics of load current. At the same time, it receives a current to recharge the battery. The output current of the parallel converter is

$$i_p = I_1 \sin \theta + I_b + \sum I_h \quad (3.10)$$

where I_h is the harmonic current and I_b is the current for charging the battery. Phasor of I_b is perpendicular to $I_1 \sin \theta$ and their internal product is zero. Therefore, the characteristic power of the parallel converter is

$$CS_p = V_{ref} I_1 \sqrt{\sin^2 \theta + k_b^2 + THD_i^2} \quad (3.11)$$

THD_i is the total harmonic distortion of the load current and is defined as $THD_i = \sqrt{\sum I_h^2} / I_1$. k_b is also defined as

$$k_b = \frac{\text{Input power of the battery}}{\text{Apparent load power}} \quad (3.12)$$

The characteristic power of the load also includes the harmonic currents and is

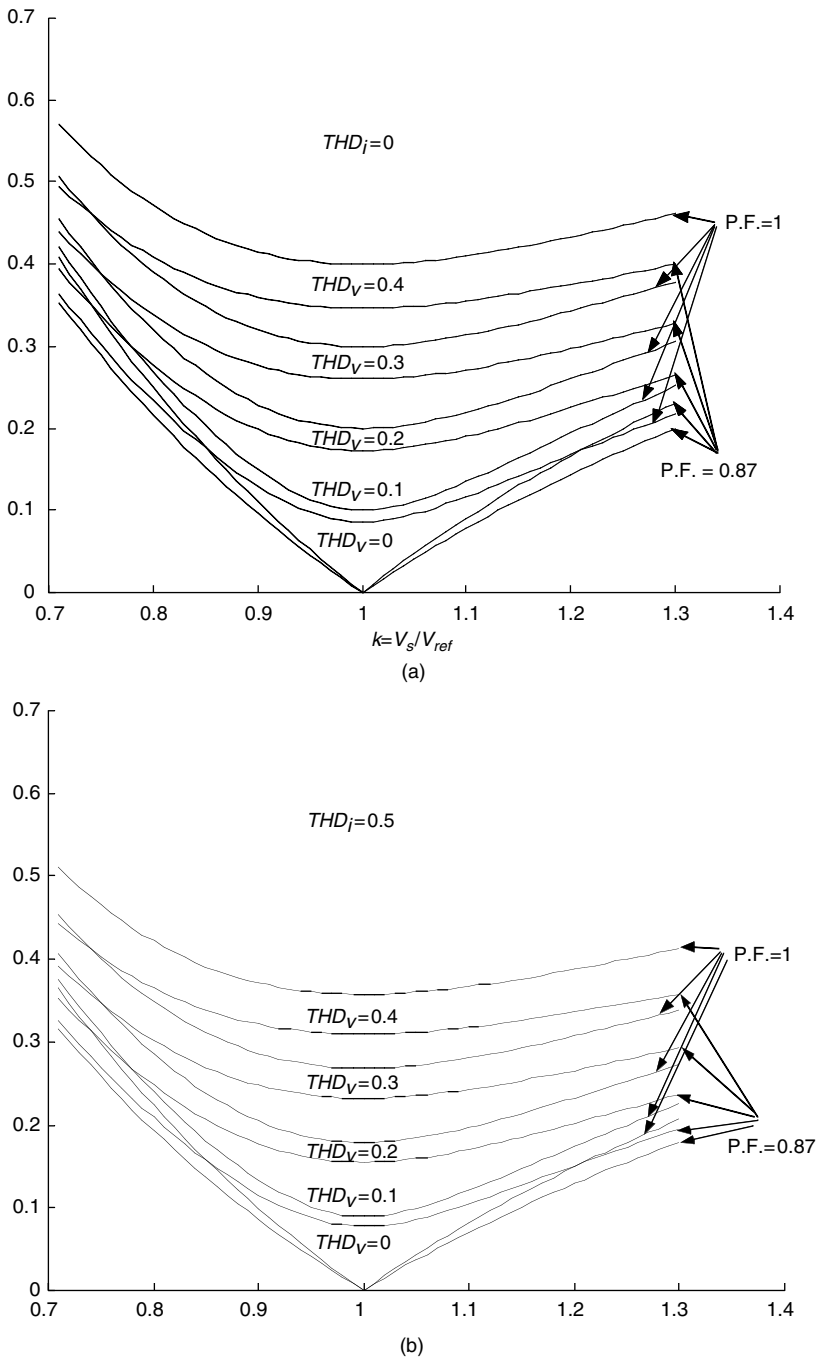
$$CS_L = V_{ref} I_1 \sqrt{1 + THD_i^2} \quad (3.13)$$

Figure 3.13 shows the characteristic power of the series converter with variation of the input voltage with different values of THD_v . These curves are used to determine the power rating of the series converter. As depicted in Figure 3.13, for instance, the rating of the series converter must be almost 35% of the characteristic power of the load for compensating a sag or swell with 30% under- or over-voltage, when THD_v is zero. In the UPQC system, these curves are also used to determine the maximum permissible voltage sag magnitude and duration. These values are also dependent on the size of the capacitor and maximum allowable voltage ripple. The maximum single-phase voltage sag duration can be achieved from the following equation:

$$t_{\max} = \frac{1/2C_{dc}(V_{dc}^2 - V_{dc\min}^2)}{CS_{\text{Series}}} \quad (3.14)$$

where $V_{dc\min}$ is the minimum permissible voltage on the DC capacitor.

The characteristic power of the parallel converter with different load power factors and THD_i is shown in Figure 3.14. In the UPQC system, these curves are used to determine the power rating of the parallel converter. In the UPS system, in the backup mode, the parallel converter supplies the load. Therefore, it must be rated at 100% of the load apparent power.

**FIGURE 3.13**

Characteristic power of the series converter (CS_{series}/CS_L vs. $k = V_s/V_{ref}$): (a) $THD_i = 0$, and (b) $THD_i = 50\%$.

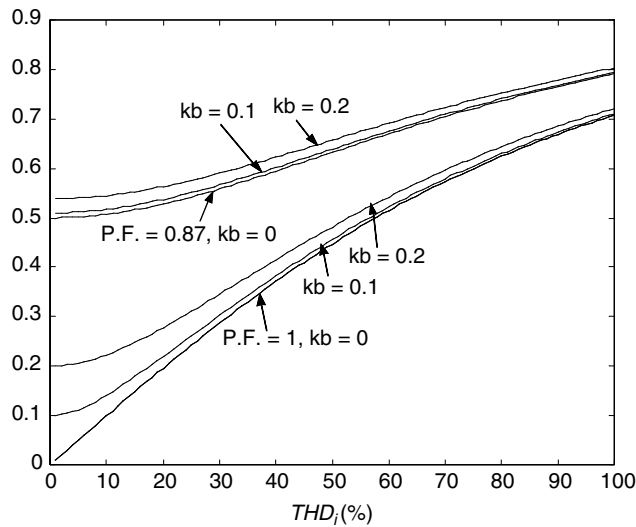


FIGURE 3.14
Characteristic power of the parallel converter (CS_p/CS_L).

Typical experimental results are shown in Figure 3.15, Figure 3.16, Figure 3.17 and Figure 3.18. The experimental results have been obtained from a 1.3 kW experimental test setup system. The current and voltage controllers have been constructed digitally using a TMS320LF2407 digital signal processor (DSP) [10]. The load is a 1 kW inductive three-phase diode rectifier. The voltage of the DC bus is 440 V. The parameters of the system are shown in Table 3.1. Figure 3.15 shows the current harmonics compensation of the parallel converter. Voltage sag, swell, and harmonics compensation in the UPS system are shown in Figure 3.16. Voltage harmonic cancellation in UPQC

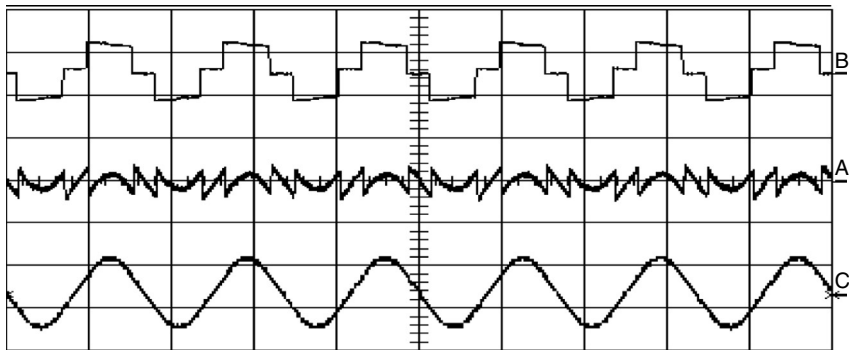
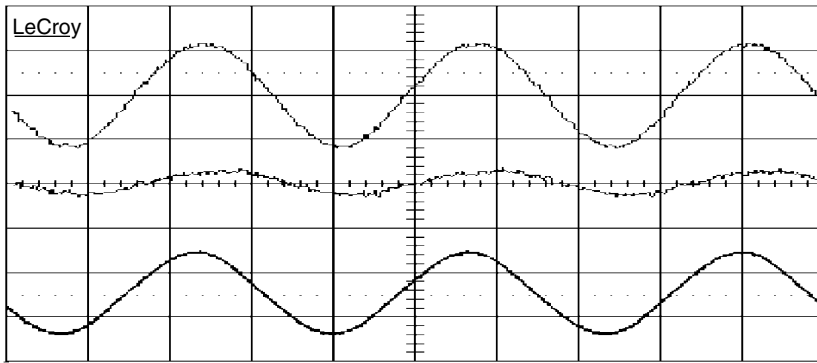
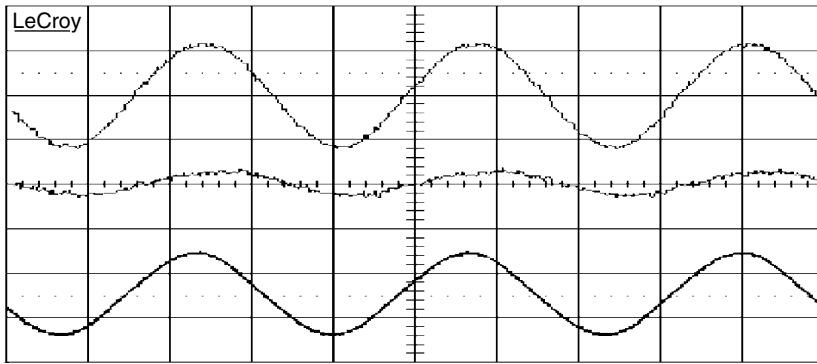


FIGURE 3.15
Typical experimental results of the parallel converter, from top to bottom: current of load, parallel converter, and line (X-axis 10 ms/div, Y-axis 4 A/div).



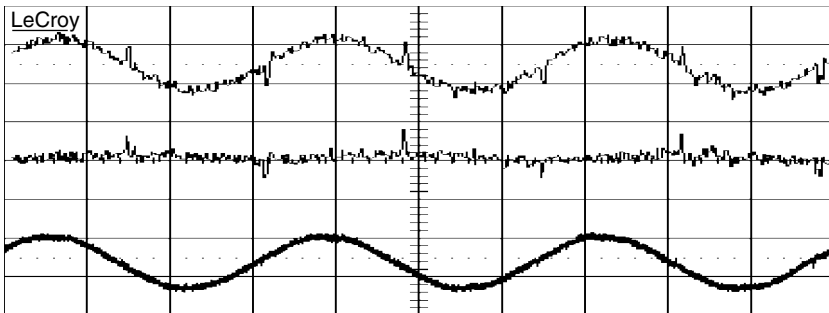
(a)



(b)

FIGURE 3.16

Typical experimental results of the series converter in a UPS system, from top to bottom: voltage of line, series converter, and load: (a) voltage sag compensation, and (b) voltage swell and harmonics compensation (X-axis 5 mS/div, Y-axis 150 V/div).

**FIGURE 3.17**

Typical experimental results of the series converter in UPQC system for voltage harmonic compensation, from top to bottom: voltage of line, series converter, and load (X-axis 5 mS/div, Y-axis 200 V/div).

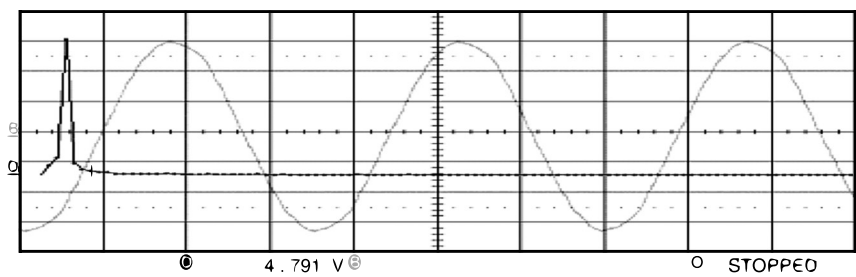


FIGURE 3.18 Typical experimental results of the UPS system in backup mode: load voltage and its frequency spectrum (X-axis 5 mS/div, Y-axis 50 V/div).

TABLE 3.1
Parameters of the experimental test setup

P_{Load}	C_{dc}	L_1	C_1	L_2	C_2
1.3 kW	1360 μ F	1 mH	4.7 μ F	0.1 mH	2.7 μ F

is shown in Figure 3.17. The voltage of the load terminal and its frequency spectrum in the backup mode of the UPS system are shown in Figure 3.18. The achieved THD of the load voltage is less than 3%.

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4

Reduced-Parts Uninterruptible Power Supplies

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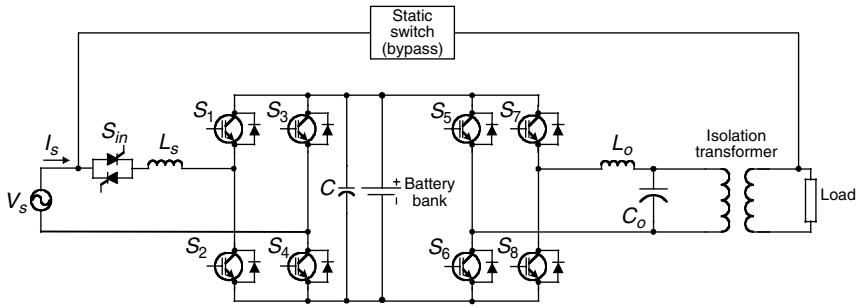
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The advances in power electronics during the past two decades have resulted in a great variety of new topologies and control strategies for uninterruptible power supply (UPS) systems. Research has focused mainly on improving the performance and expanding the application areas of the UPS systems. The issue of reducing the cost of converters has recently been attracting the attention of researchers [1–11]. Generally, the largest cost reduction is achieved by reducing the number of switches employed in a converter power circuit. Another way of reducing the cost of converters is to use a topology that allows replacing active switches, such as IGBTs, MOSFETs, and thyristors, with diodes. Diodes are less expensive than active switches and apart from this, there is also a cost reduction from eliminating all the circuitry for driving active switches. Cost reduction is also possible by developing topologies that employ switches with lower voltage stresses. Finally, cost reduction of converters is achievable by eliminating passive components such as inductors, capacitors, and transformers.

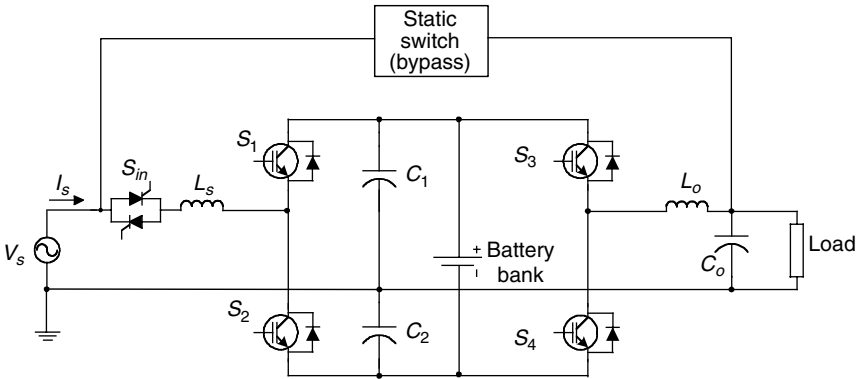
Reducing the number of switches and passive elements in UPS topologies not only reduces the cost of the whole system but also provides some other advantages such as greater compactness, smaller weight, and higher reliability. Eliminating some of the switches or replacing active switches with diodes usually complicates circuit topology and reduces the degrees of freedom in the control strategy. As a result, the control is usually more sophisticated. However, modern digital signal processor (DSP) controllers can perform the task with no added cost associated with the more complicated control.

4.1 Concept of Reduced-Parts Converters Applied to Single-Phase On-Line UPS Systems

A typical single-phase on-line UPS system based on full-bridge converters is shown in [Figure 4.1](#).

**FIGURE 4.1**

Typical single-phase on-line UPS system based on full-bridge converters.

**FIGURE 4.2**

Typical single-phase on-line UPS system based on half-bridge converters.

Applying the concept of reduced-parts converters to the UPS system based on full-bridge converters naturally leads to the UPS system based on half-bridge converters shown in Figure 4.2.

The UPS system based on full-bridge converters has some advantages over the one based on half-bridge converters, such as: better utilization of the DC-link voltage, two times lower voltage stresses across the switches, and an option of zero state for the switches, which allows using more advanced control strategies. These advantages make the UPS system from Figure 4.1 the preferable choice for medium- and high-power applications. However, the disadvantage is that it has a large number of switches. It also requires an isolation transformer at the back-end, which is bulky, heavy, and expensive. This is why the UPS system based on half-bridge converters from Figure 4.2 is the preferable choice for low-power applications. It not only has two times lower the number of switches than the UPS topology from Figure 4.1

but it also has a common neutral for the input and the output, eliminating the need for an isolation transformer.

One of the most important features of UPS systems is their reliability and availability. The component that influences these characteristics most considerably is the battery. As mentioned previously, there are two options for connecting batteries in UPS systems. The first is to connect them directly in parallel with the DC-link capacitors, which leads to several problems, such as: space, cost, reliability, and safety issues. The second is to add a bidirectional DC/DC converter [8, 9]. An on-line UPS system, based on half-bridge converters using a bidirectional DC/DC converter, is shown in Figure 4.3.

During the normal mode of operation, the buck converter charges the battery bank and at the same time the power to the load is continuously supplied from the AC line through the rectifier, to the inverter, and finally to the load. Switches S_1 to S_5 are active, while switch S_6 is idle.

During the stored-energy mode of operation, when the AC input voltage is beyond a preset tolerance, switch S_{in} disconnects the UPS system from the grid. The DC/AC inverter and the battery bank maintain continuity of power to the load. Since the battery voltage is low, it first requires to be boosted to a high DC voltage for proper operation of the DC/AC inverter. Switch S_6 is active during this operation mode as well as the inverter's switches S_3 and S_4 . The rectifier does not work during this mode and its switches S_1 and S_2 are idle.

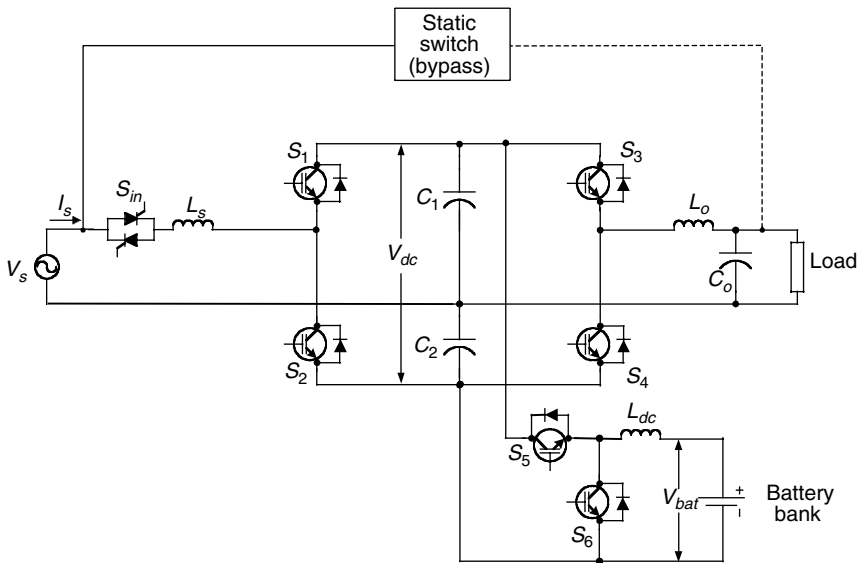


FIGURE 4.3

Typical single-phase on-line UPS system based on half-bridge converters with bidirectional DC/DC converter.

4.2 New On-Line UPS Systems Based on Half-Bridge Converters

In this section, three new reduced-parts on-line UPS systems, based on half-bridge converters, are presented and their operating principles are explained. The design considerations for 1 kVA prototypes are outlined and the results of extensive computer simulations are presented.

4.2.1 Reduced-Parts Single-Phase On-Line UPS System

Careful consideration of the UPS system, from Figure 4.3, reveals that switch S_6 can be eliminated, as long as the low battery voltage can be boosted to a high DC voltage. Taking advantage of the fact that the AC/DC rectifier is of a boost type and it is not in use during the stored-energy mode of operation, it is possible to eliminate switch S_6 by changing the topology of the UPS system from Figure 4.3 in such a way that the rectifier leg is used as a part of a DC/DC boost converter during the stored-energy mode of operation. Apart from eliminating switch S_6 , the use of the rectifier as a boost DC/DC converter during the stored-energy mode of operation relaxes the current rating requirements for the inductor in the DC/DC converter. As a result, the inductor is significantly smaller, lighter, and less expensive. The proposed new single-phase on-line UPS system with a reduced number of switches is shown in Figure 4.4.

4.2.1.1 Description of the Proposed UPS System

The new UPS system, shown in Figure 4.4, has a front-end AC/DC rectifier with power factor correction capabilities, a DC/AC inverter, a step-down DC/DC converter, a battery bank, an input switch S_{in} , a transfer switch S_t in

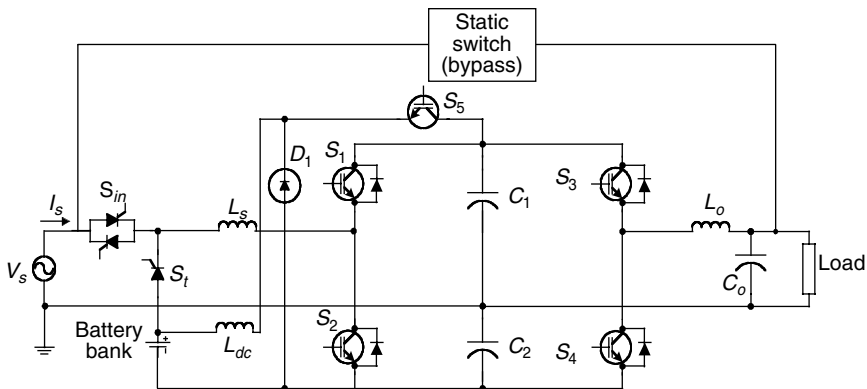


FIGURE 4.4

Proposed new single-phase on-line UPS system with reduced number of switches.

the form of a thyristor, and a bypass static switch. The AC/DC rectifier consists of an input inductor L_s , switches S_1 and S_2 , and two electrolytic capacitors C_1 and C_2 . The purpose of the rectifier is to keep the input current sinusoidal and in phase with the input AC voltage, while maintaining the required DC bus voltage at a level necessary for proper operation of the back-end inverter. The DC/AC inverter consists of a split DC bus, and switches S_3 and S_4 , as well as an output LC filter. It operates in a high-frequency sinusoidal pulse width modulation (SPWM) pattern in order to provide a high-quality sinusoidal output voltage.

The DC/DC buck converter consists of switch S_5 , diode D_1 , and DC inductor L_{dc} . Its purpose is to step down the high DC bus voltage to a low battery voltage, thus controlling the charge of the battery bank. The input switch S_{in} disconnects the UPS system from the grid in the stored-energy mode of operation in order to prevent back feeding of power from the battery bank to the grid. The transfer switch S_t is used to transfer the input power source from the AC line to the battery. The bypass static switch is used to “bypass” the UPS system in case of UPS failure or if maintenance is required. The output frequency must be the same as the AC line frequency in order to ensure transfer from the normal to the bypass mode and vice versa.

4.2.1.2 Basic Principles of Operation

The proposed UPS system has three operating modes: normal mode, stored-energy mode, and bypass mode. In the normal mode of operation, the input AC voltage is within the permissible tolerance range. The power is passed from the AC/DC rectifier to the DC/AC inverter and the load is continuously supplied with high-quality AC power. The buck converter maintains the battery bank at 100% state of charge. The transfer switch S_t is off.

The front-end rectifier works in the following way. During the positive half cycle of the input AC voltage, when switch S_2 is on, the expression for the voltage across the input inductor L_s is derived from the second Kirchhoff's law:

$$V_{L_s} = L_s \frac{di_s}{dt} = V_s + V_{C_2} \quad (4.1)$$

The voltage applied across the input inductor is positive; hence, the inductor current increases. The current path during this time is $V_s^+ - L_s - S_2 - C_2 - V_s^-$. The corresponding circuit is shown in [Figure 4.5](#).

When switch S_2 is turned off, the inductor current needs to continue flowing in the same direction. The only possible current path in this case is $V_s^+ - L_s$ —reverse diode of $S_1 - C_1 - V_s^-$. The upper capacitor C_1 is charged with the energy stored in inductor L_s . The voltage across the input inductor L_s is

$$V_{L_s} = L_s \frac{di_s}{dt} = V_s - V_{C_1} \quad (4.2)$$

Since V_{C_1} is larger than V_s , the voltage applied across the input inductor is negative and the inductor current decreases. The corresponding circuit is

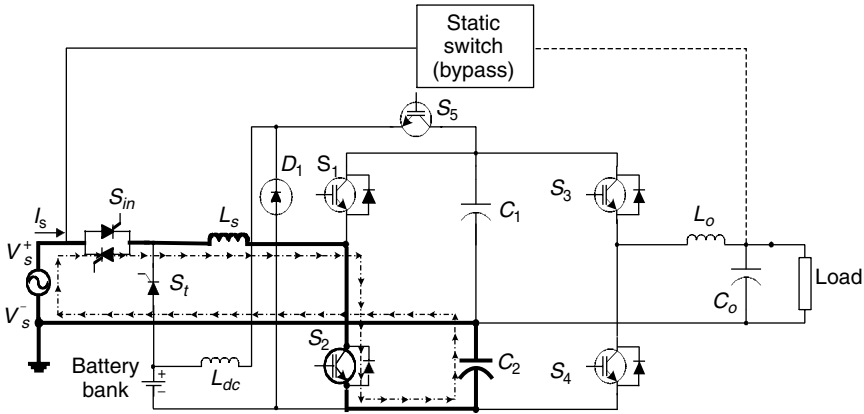


FIGURE 4.5

Corresponding circuit diagram for the positive half-cycle of the input voltage with S_2 closed.

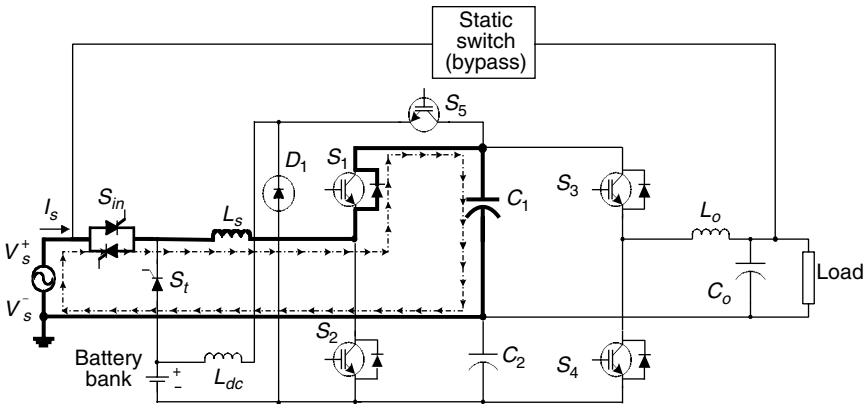


FIGURE 4.6

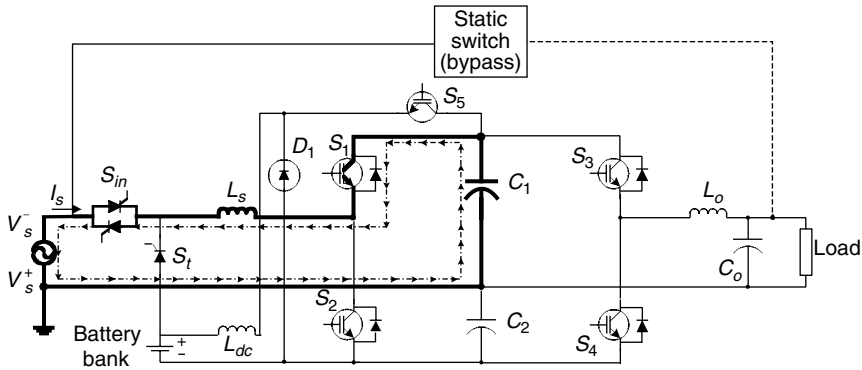
Corresponding circuit diagram for the positive half-cycle of the input voltage with S_2 open.

shown in Figure 4.6. In this way, during the positive half-cycle of the input voltage, the input power factor and the DC voltage of the upper capacitor C_1 are controlled by the duty ratio of switch S_2 .

During the negative half-cycle of the input AC voltage, when switch S_1 is on, the voltage across the input inductor L_s is negative as shown in Equation 4.3.

$$V_{L_s} = L_s \frac{di_s}{dt} = -V_s - V_{C_1} \quad (4.3)$$

Since the voltage applied across the input inductor is negative, the inductor current decreases. During that time, energy is stored in the current shaping inductor L_s , which is transferred to the bottom capacitor C_2 when switch S_1 is turned off. The current path during the time when S_1 is on is $V_s^+ - C_1 - S_1 - L_s - V_s^-$. The corresponding circuit is shown in Figure 4.7.

**FIGURE 4.7**

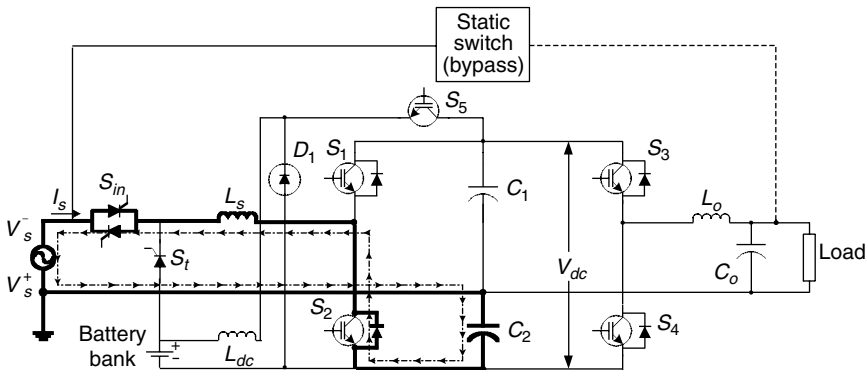
Corresponding circuit diagram for the negative half-cycle of the input voltage with S_1 closed.

When switch S_1 is turned off, the inductor current needs to continue flowing in the same direction. The current path in this case is $V_s^+ - C_2$ —reverse diode of $S_2 - L_s - V_s^-$. Therefore, the bottom capacitor C_2 is charged with the energy stored in inductor L_s . The voltage across the input inductor L_s is

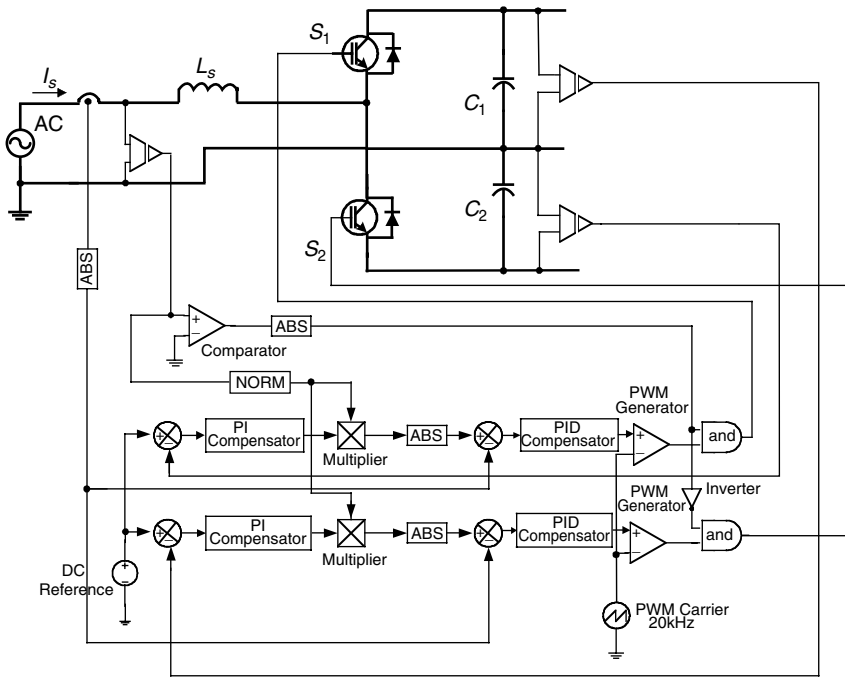
$$V_{L_s} = L_s \frac{di_s}{dt} = -V_s + V_{C_2} \quad (4.4)$$

Since V_{C_2} is larger than V_s , the voltage applied across the input inductor is positive and the inductor current increases. The corresponding circuit is shown in Figure 4.8. In this way, during the negative half-cycle, the input power factor and the DC voltage of the bottom capacitor C_2 are controlled by the duty ratio of the upper switch S_1 .

A diagram of the implemented control is shown in Figure 4.9. The control strategy for the AC/DC rectifier uses multiple control loops for each switch: one outer voltage loop and one inner current loop. The outer

**FIGURE 4.8**

Corresponding circuit diagram for the negative half-cycle of the input voltage with S_1 open.

**FIGURE 4.9**

Control strategy for the AC/DC rectifier.

control loop uses the voltage of the output DC-link capacitor as a feedback signal, which is compared with a reference signal. A *PI* integrator compensates the error. The output of the *PI* integrator is used as a reference signal for the inner current regulator loop, which uses the input inductor current as a feedback signal. The minor current loop is fast and gives good dynamic response, resulting in a very good input power factor. The outer voltage loop is slower and keeps the output DC-link voltage stable at 480 V: 240 V for each capacitor C_1 and C_2 . The switching frequency is 20 kHz.

The step-down DC/DC converter charges the battery bank in the following manner. When switch S_5 is turned on, the voltage across DC inductor L_{dc} is positive:

$$V_{L_{dc}} = L_{dc} \frac{di}{dt} = V_{dc} - V_{bat} \quad (4.5)$$

The current through inductor L_{dc} increases and charges the battery bank. When switch S_5 is turned off, the inductor voltage $V_{L_{dc}}$ is negative, as shown in Equation 4.6 and the inductor current decreases, flowing through $L_{dc} - V_{bat} - D_1$.

$$V_{L_{dc}} = L_{dc} \frac{di}{dt} = -V_{bat} \quad (4.6)$$

This way, the high DC voltage is stepped down to low battery voltage by switching switch S_5 on and off. The battery voltage is directly proportional to the duty ratio D of S_5 , as shown in Equation 4.7.

$$V_{bat} = D \times V_{dc} \quad (4.7)$$

Figure 4.10 shows the voltage across diode D_1 , the current through inductor L_{dc} and output voltage V_{out} across the battery terminals [12].

The DC/AC inverter is a half-bridge type, consisting of two DC capacitors C_1 and C_2 , connected in series, two switches S_3 and S_4 , and an output LC filter. The input DC voltage V_{dc} is equally divided between the two capacitors. By turning switches S_3 and S_4 on and off, the voltage applied across the load is $+V_{dc}/2$ or $-V_{dc}/2$. When switch S_3 is on, switch S_4 is off and the load voltage is $+V_{dc}/2$. Also, when switch S_3 is on, switch S_4 is off and the load voltage is $-V_{dc}/2$. To avoid shoot-through faults, there is always a dead band between the time when one of the switches is turned off and the other is turned on. The duration of the dead band should be large enough to allow the switch that is turned off to close before the other switch starts conducting. The DC/AC inverter operates in a high-frequency SPWM pattern in order to provide a high-quality sinusoidal output voltage.

A diagram of the implemented SPWM control strategy for the DC/AC inverter is shown in Figure 4.11. The control strategy employs two control loops: one outer voltage loop and one inner current loop. The outer control loop uses the output voltage as a feedback signal, which is compared with a reference signal. The error is compensated by a PI compensator to achieve a

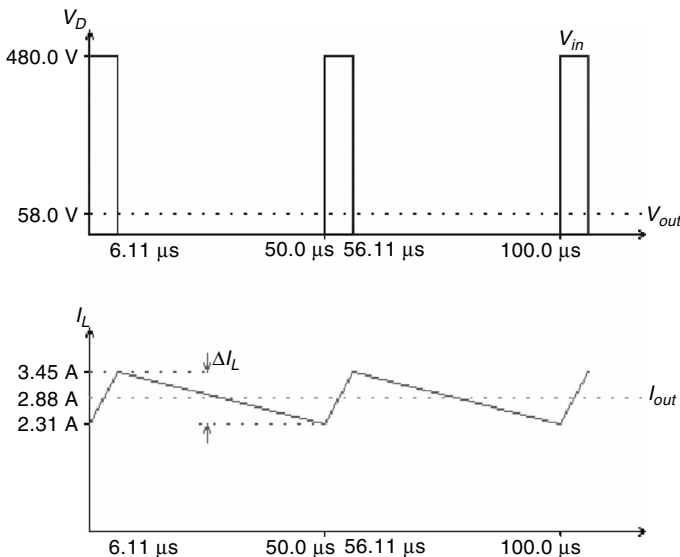
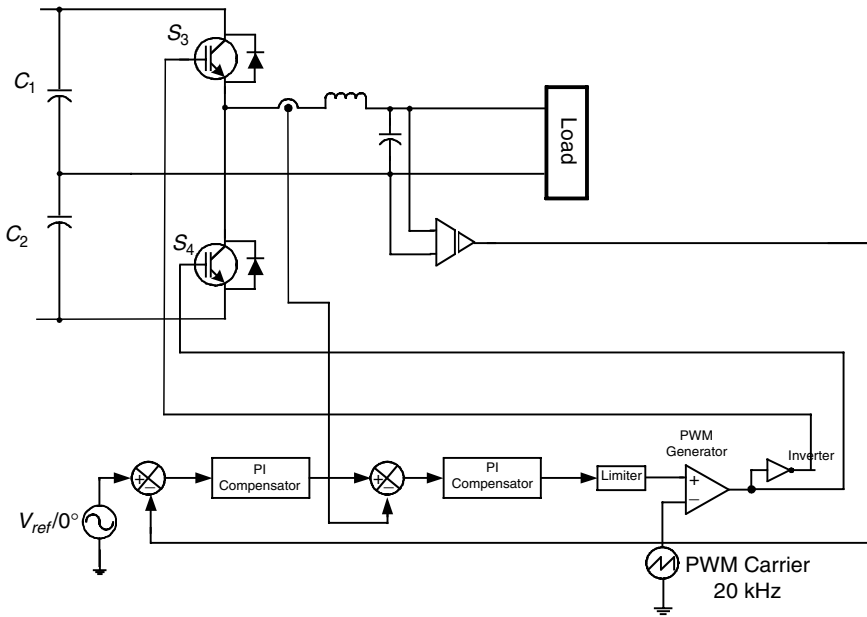


FIGURE 4.10

Operation of the DC/DC step-down converter.

**FIGURE 4.11**

Control strategy for the DC/AC inverter.

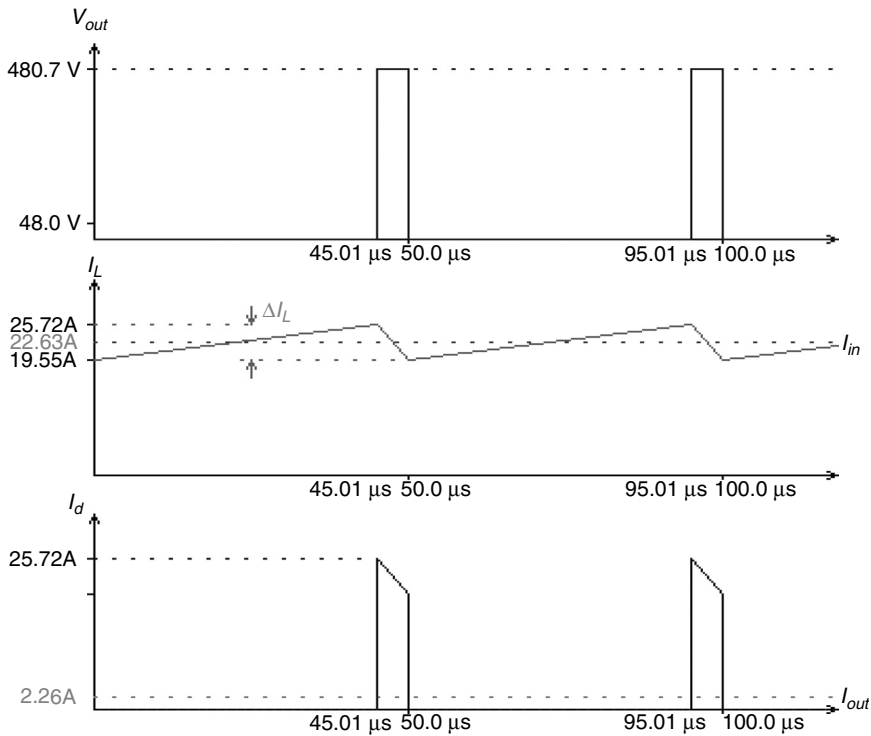
stable output voltage under steady-state operation. This error is also used as a reference signal for the inner current regulator loop, which uses the output current as a feedback signal. The minor current loop is much faster than the outer voltage loop and improves the dynamic response of the inverter. As a result, the output voltage has a very high quality even with a highly nonlinear load. The switching frequency is 20 kHz.

In the stored-energy mode of operation, when the input AC voltage is beyond the permissible tolerance range, switch S_{in} is turned off and switch S_i is turned on, transferring the input from the AC line to the battery bank. Since the battery voltage is low, it first requires to be boosted to high DC voltage for proper operation of the DC/AC inverter.

The boost DC/DC converter consists of switch S_2 , the reverse diode of switch S_1 , inductor L_s , and capacitors C_1 and C_2 . When switch S_2 is turned on, the low input battery voltage is applied across L_s . The positive voltage across inductor L_s causes the inductor current to increase. The current path is $V_{bat}^+ - L_s - S_2 - V_{bat}^-$. When switch S_2 is turned off, the current path is $V_{bat}^+ - L_s$ —reverse diode of S_1 — C_1 — C_2 — V_{bat}^- and the current buildup in L_s charges capacitors C_1 and C_2 . In this way, the low battery voltage V_{bat} is boosted to the high DC voltage V_{dc} by turning switch S_2 on and off:

$$V_{dc} = \frac{V_{bat}}{1-D} \quad (4.8)$$

where D is the duty ratio of switch S_2 .

**FIGURE 4.12**

Operation of the DC/DC step-up converter.

Figure 4.12 shows the voltage across switches S_2 , output voltage V_{out} across the DC-link bus, the current through inductor L_s , and the current through the reverse diode of S_1 [12].

The operation of the DC/AC inverter in the stored-energy mode is the same as that in the normal operating mode.

4.2.1.3 Design of a 1 kVA UPS System

An experimental setup has been designed with the following parameters:

- Input voltage: Single-phase 120 VAC $\pm 25\%$
- Battery voltage: 48 V
- DC-link bus voltage: 480 V (2×240 V)
- Output voltage: Single-phase 120 VAC $\pm 5\%$
- Output frequency: 60 Hz $\pm 0.5\%$
- THD: $< 5\%$
- Output power: 1 kVA continuous
- Switching frequency: 20 kHz

The power output for the UPS system is 1000 W. Assuming an efficiency of 85%, the input power P_{in} is calculated as

$$P_{in} = \frac{P_{out}}{\eta} = \frac{1000}{0.85} = 1176.5 \text{ W} \quad (4.9)$$

The minimum RMS input voltage is $V_{in_{min}} = 85 \text{ V}$. The maximum input current $I_{in_{max}}$ is drawn at the minimum input voltage and maximum load and is calculated as shown in Equation 4.10:

$$I_{in_{max}} = \frac{P_{in}}{V_{in_{min}}} = \frac{1176.5}{85} = 13.84 \text{ A} \quad (4.10)$$

The IGBTs for the front-end rectifier and the back-end inverter need to carry at least two times the $I_{in_{max}}$ in order to provide the inrush current for loads that require this at their start-up. IGBTs with a current rating of 50 A have been selected in order to provide sufficient safe margins.

The voltage across each DC-link capacitor is 240 V, and the total voltage of the DC-link bus is 480 V. This is the voltage stress across each IGBT in the UPS system from Figure 4.4. IGBT modules with a voltage rating of 600 V and current rating of 50 A have been chosen for active switches for the AC/DC rectifier and the DC/AC inverter. The CM50DY-12H modules from Powerex are specifically designed for high switching frequency applications. Each module consists of two IGBTs in a half-bridge configuration, with each transistor having a reverse-connected, superfast recovery freewheeling diode. All components and interconnects are isolated from the heat sinking base plate, offering a simplified system assembly and thermal management. The circuit layout of the IGBT module is shown in Figure 4.13.

The active switch for the step-down converter needs to carry the maximum battery charging current and withstand the DC-link bus voltage of 480 V. A standard 48 V battery kit for a 1 kVA UPS system has been used. It is a set of four 12 V-7.2 Ah batteries, Panasonic LC-P127R2P, connected in series. The manufacturer specifies the constant voltage charging method with an initial charging current of 2.88 A or smaller and a control voltage of 14.5 to 14.9 V per 12 V cell at 25°C. An International Rectifier IGBT, with part number

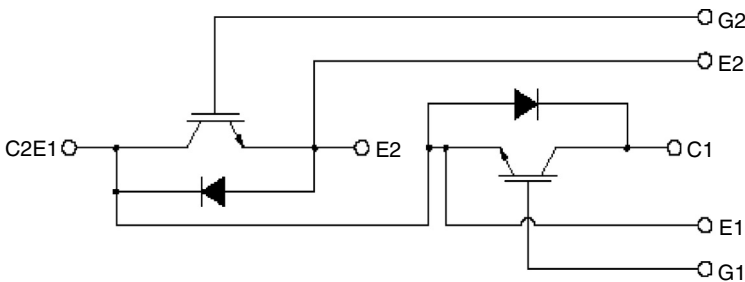


FIGURE 4.13

Circuit diagram of the Powerex IGBTMOD™ module.

IRG4BC20K, has been selected with a voltage rating of 600 V and a current rating of 20 A. The freewheeling diode in the step-down converter needs to be an ultrafast type and should have the same voltage and current rating as the IGBT. An International Rectifier ultrafast diode, with part number 30EPH06, has been selected with a voltage rating of 600 V and a current rating of 30 A.

To determine the optimum value of the current shaping inductor, for a fixed frequency power factor correction (PFC) converter, several trade-offs should be considered, such as: peak current vs. average current and switching losses vs. core losses. All of these parameters are functions of the input voltage, load, and inductance, and effectively determine whether the PFC converter works in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). The CCM of operation is widely recognized as the superior one for PFC converters with a power rating above 500 W. Accordingly, a design procedure for the input current shaping inductor was adopted, which ensures that the converter would work in CCM. The inductance value that would cause the input ripple current to be a fraction of the overall input current is given in Equation 4.11 and is calculated in Equation 4.12 as

$$L_s = \frac{T \times V_{in_{min}}^2}{2 \times I\% \times P_{out}} \left(1 - \frac{\sqrt{2} \times V_{in_{min}}}{V_{dc}} \right) \quad (4.11)$$

$$L_s = \frac{50 \times 85^2}{2 \times 0.35 \times 1176.5} \left(1 - \frac{\sqrt{2} \times 85}{480} \right) = 329 \mu\text{H} \quad (4.12)$$

where L_s is the inductance (μH), T is the switching period (μs), $V_{in_{min}}$ is the minimum RMS input voltage (V), $I\%$ is the percent switching current ripple relative to the input current, P_{out} is the maximum output power (W), and V_{dc} is the output DC voltage (V).

A value of 350 μH has been chosen for L_s to provide sufficient safe margins for rolloff of the inductance at high frequency and heavy load. Magnetic Inductor Design Software from Magnetics® has been used to design the inductor. A stack of two high flux powder cores 58908-A2 with 77 turns of two parallel strands of 12 AWG copper wire gives an inductance of 357.56 μH at full load and 438.75 μH at no load. The core losses are calculated to be 0.7 W and the copper losses are 26.7 W, which yields a temperature rise of 44.7°C.

The selection of the DC-link capacitors C_1 and C_2 is determined by the voltage ripple specifications and the AC current for each capacitor [13]. The inverter output current is expected to contain a fundamental harmonic as well as higher harmonic components due to nonlinear loads. It can be expressed as

$$i_o(t) = \sqrt{2} I_1 \sin(\omega_1 t - \phi_1) + \sqrt{3} I_3 \sin(\omega_3 t - \phi_3) + \dots \quad (4.13)$$

For simplicity, if we assume that the inverter output current consists of a fundamental component and third harmonic only, and assuming that the third harmonic is 70% of the value of the fundamental, which is typical for a single-phase rectifier, then for the inverter output current, we have

$$I_o = \sqrt{I_1^2 + I_3^2} = 1.22 I_1 \quad (4.14)$$

The nominal inverter output current is 8.33 A as

$$I_o = \frac{P_o}{U_o} = \frac{1000}{120} = 8.33 \text{ A} \quad (4.15)$$

The fundamental frequency current is given by

$$I_1 = \frac{I_o}{1.22} = \frac{8.33}{1.22} = 6.83 \text{ A} \quad (4.16)$$

The largest AC component of the DC-link capacitor current is half the fundamental frequency current, whose RMS value is

$$i_{c,rms} = \frac{1}{2} I_1 = \frac{1}{2} 6.83 = 3.415 \text{ A} \quad (4.17)$$

Specifying voltage ripples ΔV_c of less than 1% or 2.4 V, we calculate the value for capacitors C_1 and C_2 according to

$$\Delta V_c = \frac{i_{c,rms}}{\omega C} = \frac{i_{c,rms}}{2\pi C} \quad (4.18)$$

$$C = \frac{i_{c,rms}}{\omega \Delta V_c} = \frac{3.415}{2\pi \times 60 \times 2.4} = 3776 \text{ } \mu\text{F} \quad (4.19)$$

Approximately 1000 μF higher value capacitors have been chosen in order to provide sufficient holdup time. The holdup time is necessary to maintain the load running during the time that the system needs to sense that the input voltage is beyond tolerance and effectively transfer the energy source from the AC line to the battery bank. The excess capacitance also reduces the voltage ripples, which improves the performance of the DC/AC inverter. Two electrolytic capacitors (United Chemi-Con® 36DA472F250BF2A) have been selected with a 250 V voltage rating and a capacitance of 4700 μF .

The maximum allowable percent of current ripples in the inductor in the step-down DC/DC converter determines the minimum value of inductance for L_{dc} . The inductance value for L_{dc} is calculated as

$$L_{dc} = \left(\frac{V_{dc} - V_{bat}}{\Delta I_L} \right) \times \frac{D}{f} \quad (4.20)$$

$$L_{dc} = \left(\frac{480 - 58}{1.15} \right) \times \frac{0.12}{20000} = 2.22 \text{ mH} \quad (4.21)$$

where V_{dc} is the DC-link voltage (V), V_{bat} the battery voltage (V), ΔI_L the inductor current ripples (A), D the duty ratio, and f the switching frequency (Hz).

A Kool Mμ powder core 77091-A7, with 292 turns of 18 AWG copper wire, yields an inductance of 2.244 mH at full load and 3.154 mH at no load. The core losses are calculated to be 135.9 W and the copper losses are 4.3 W, which yields a temperature rise of 21.7°C. The Kool Mμ powder core 77091-A7 costs \$5.42 and weighs 0.123 kg.

It is worth mentioning that the current rating for inductor L_{dc} is the maximum charging current specified by the manufacturer of the battery used. For a typical battery pack used in a 1 kVA on-line UPS system, the initial charging current is 2.88 A or smaller. This is a substantially smaller value than the current rating for inductor L_{dc} in a bidirectional DC/DC converter from Figure 4.3, which is 22.63 A. To design an inductor with 2.2 mH inductance rated at 22.63 A, the required core is Honeywell® AMCC-200, which costs \$72.50 and weighs 1.67 kg.

The pulse width modulation (PWM) output V_{in} from the IGBT leg is filtered by a low-pass LC filter shown in Figure 4.14. The cut-off frequency of the filter is set around 1.5 kHz in order to eliminate the high-frequency harmonic content of V_{in} . The filter components are selected using Equation 4.22.

$$f_c = \frac{1}{2\pi\sqrt{L_o C_o}} = 1.5 \text{ kHz} \quad (4.22)$$

The output inductor has been selected to be $L_o = 100 \mu\text{H}$ and the output capacitor to be $C_o = 20 \mu\text{F}$. Two 10 $\mu\text{F}/250 \text{ V}$ metal film 106MWR250K capacitors from Illinois Capacitor, Inc. connected in parallel have been used for the capacitor C_o .

To design the inductor L_o , Magnetic Inductor Design Software has been used. A Kool Mu powder core 77440-A7, with 45 turns of 16 AWG copper wire, yields an inductance of 100 μH at full load and 120 μH at no load. The core losses are calculated to be 3.075 W and the copper losses are 1.7053 W, which yields a temperature rise of 31.4°C.

Digital system control is becoming increasingly popular in the power electronic industry as a consequence of automated design tools becoming more widespread. Sophisticated algorithms can be implemented and updated digitally in a much shorter period of development time compared to analog circuits. Digital circuits are also much more robust and less likely to be influenced by temperature, aging, or chip layout. A digital signal processor (DSP) was used for the control and generation of the PWM signals for the gate drivers of the IGBTs. The DSP kit used in this case was the DSP starter kit (DSK) for TMS320LF2407A from Texas Instruments, Inc. The TMS320LF2407A has integrated peripherals specifically chosen for the

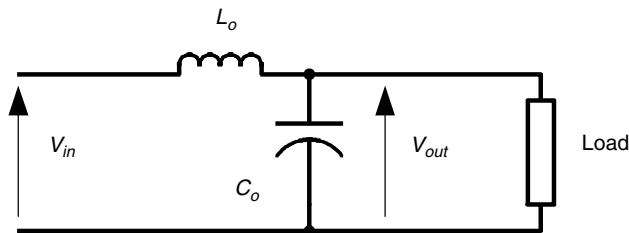


FIGURE 4.14

Low-pass LC output filter for the UPS system from Figure 4.4.

embedded control applications. These include analog-to-digital (A/D) converters, PWM outputs, timers, protection circuitry, and serial communications. Most instructions for the DSP including multiplication and accumulation (MAC) as one instruction are of a single cycle type. Therefore, multiple control algorithms can be executed at high speed, thus making it possible to achieve the required high sampling rate for good dynamic response. Digital control also introduces the advantages of programmability and immunity to noise. With fewer components, the system requires less engineering time and it can be made smaller and more reliable.

4.2.1.4 Simulation Results

Extensive computer simulations have been carried out, using PSIM simulation software, to help design the control for the new UPS system. The input AC voltage V_s and current I_s in Figure 4.15 show that the input current I_s is a sine wave in phase with the input voltage resulting in excellent power factor.

Figure 4.16 shows the DC bus voltages across capacitors C_1 and C_2 for a balanced nonlinear load.

Figure 4.17 shows the output voltage V_o and load current I_o for a balanced nonlinear load. The output voltage is a high-quality sine wave with THD less than 5%.

Figure 4.18 shows the dynamic performance of the proposed UPS system with step-changing loads. Initially, the system works at no load. After 0.10 s, a resistive load ($R=100\ \Omega$) is applied, and after another 0.10 s, an RL load ($R=30\ \Omega$ and $L=200\ \text{mH}$) is connected. As can be observed from the results, the dynamic performance of the system is excellent. No deterioration of the quality of the output voltage supplied to the critical loads has been observed. The input PF has been kept close to unity, and no stability problems have been observed.

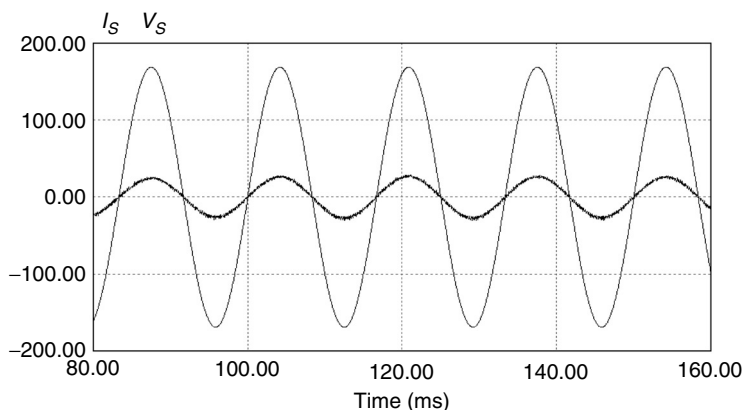


FIGURE 4.15

Input current I_s and voltage V_s .

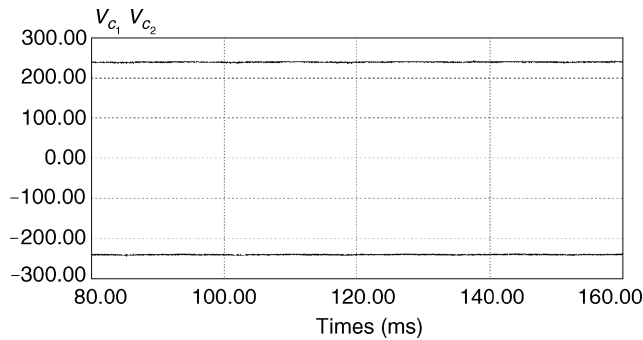


FIGURE 4.16
DC-link bus voltages for balanced nonlinear load.

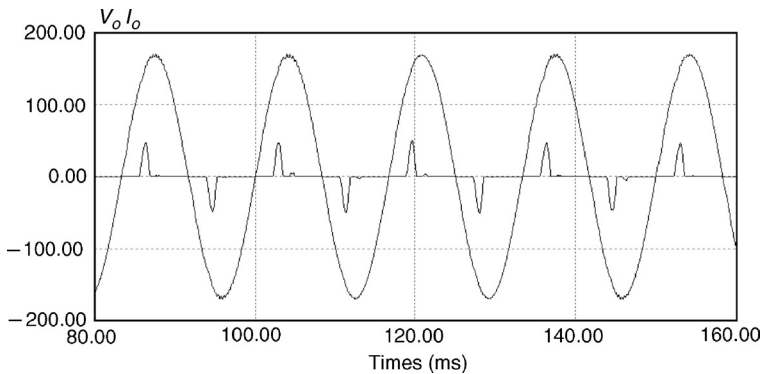
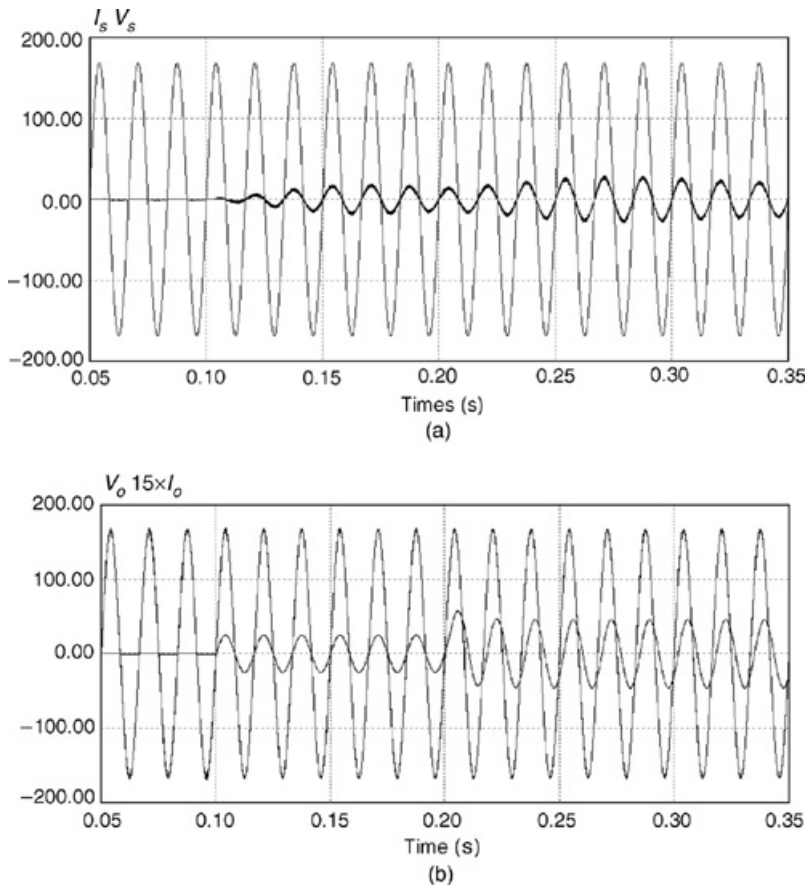


FIGURE 4.17
Output voltage V_o and current I_o .

Figure 4.19 shows the operation of the UPS system under the stored-energy mode of operation for a resistive load $R=30\ \Omega$, when the transfer switch S_i is turned on and the input energy source is the battery bank.

Figure 4.20 shows the operation of the UPS system under the normal mode of operation when the input voltage reduces from 120 to 92 V. Since the rectifier is of a boost type, the DC-link bus voltage is maintained at 480 V without the need to switch to the battery bank. This feature extends the input voltage range at which the UPS system can work in the normal operation mode. As a result, the batteries are not forced into frequent charge/discharge cycles, which in turn extends the battery life, their availability, and reliability.

Figure 4.21 shows the operation of the UPS system under the stored-energy operation mode for an unbalanced nonlinear load. The term unbalanced addresses the fact that the load draws more current during one half of the cycle than during the other half of the cycle. Such conditions can occur during the start-up of a power supply that does not have a soft start feature. Such power supplies tend to draw significant in-rush currents that are

**FIGURE 4.18**

Operation under normal operation mode with step-changing load. (a) Input voltage V_s and current I_s , and (b) output voltage V_o and current I_o .

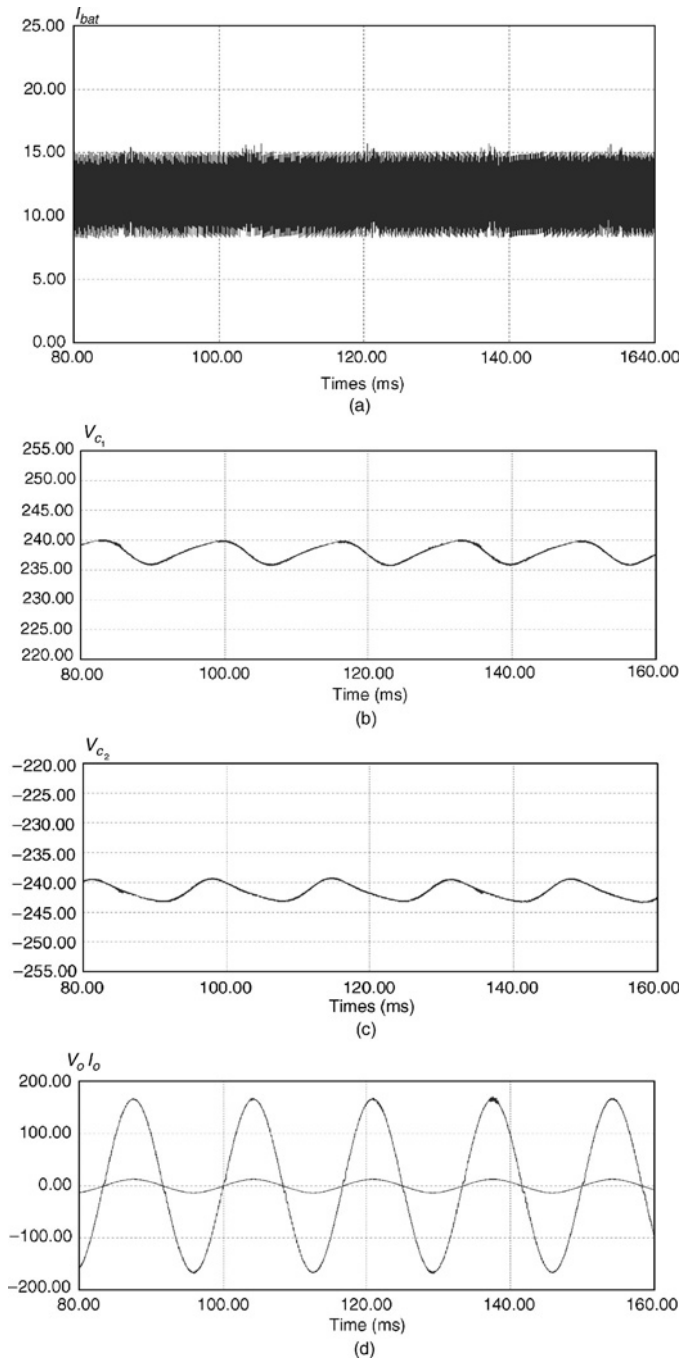
highly unsymmetrical. After the first few cycles, the DC capacitor at the back of the power supply is fully charged to the nominal operating voltage and the load becomes a symmetrical balanced nonlinear load.

4.2.2 Single-Phase to Two-Phase On-Line UPS System

A new single-phase to two-phase UPS system is derived from the UPS system described in Section 4.2 by adding one more leg to the back-end DC/AC inverter. The proposed UPS system is shown in [Figure 4.22](#).

4.2.2.1 Basic Principles of Operation

The operating principles regarding the front-end AC/DC rectifier, the DC/DC step-down converter, and the DC/DC step-up converter are the

**FIGURE 4.19**

Operation under stored-energy mode of operation for balanced nonlinear load. (a) Battery current I_{bat} , (b) DC bus voltage V_{C1} , (c) DC bus voltage V_{C2} and (d) output voltage V_o and current I_o .

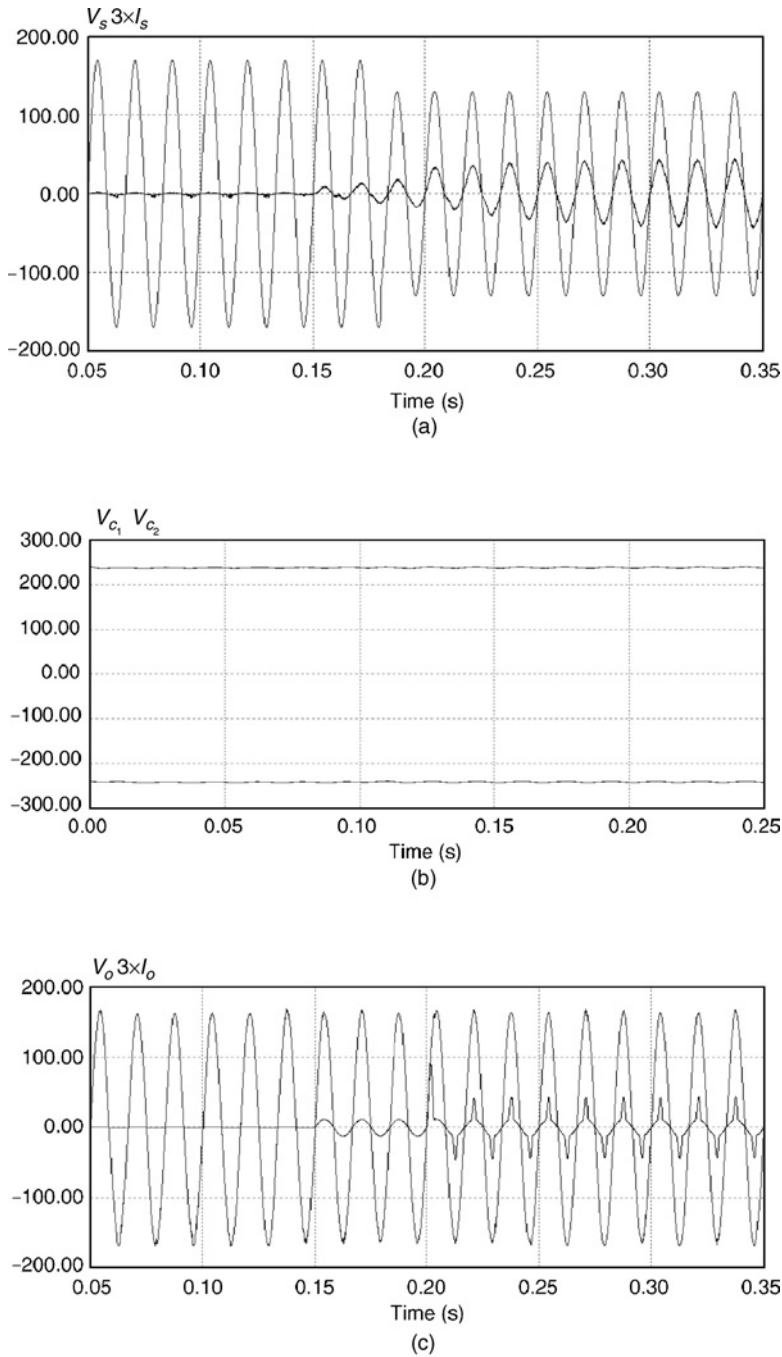
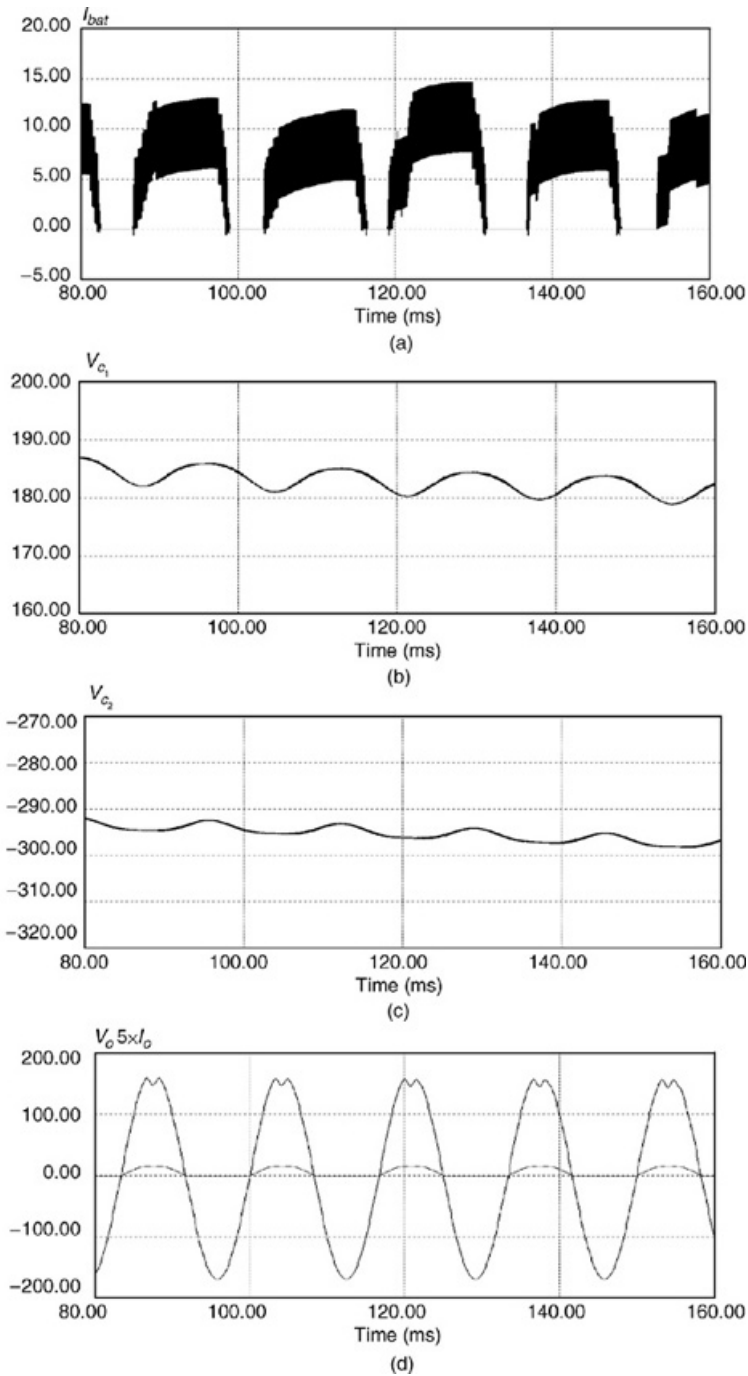
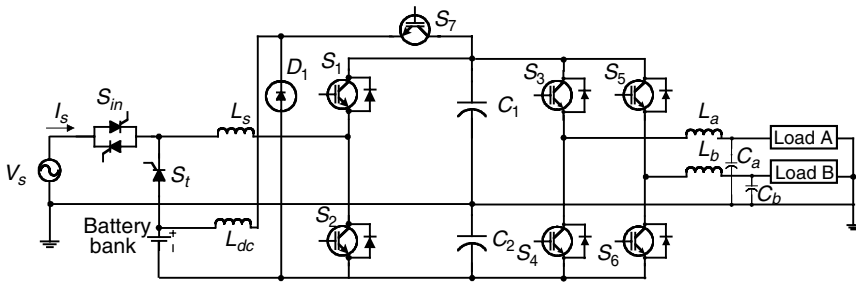


FIGURE 4.20

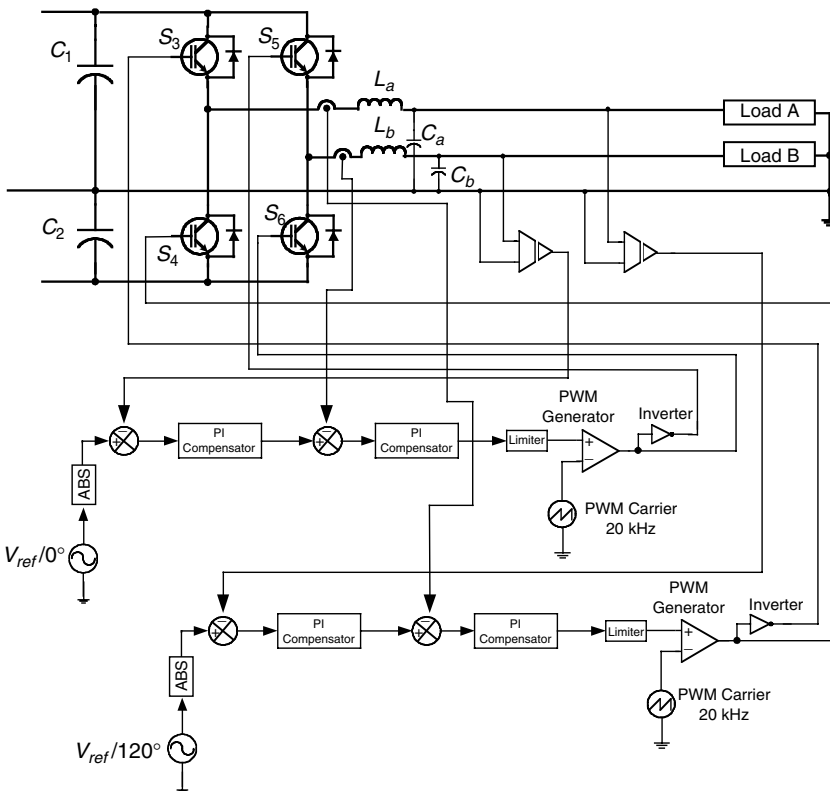
Operation under normal mode of operation with input voltage S_{ag} . (a) Input voltage V_s and current I_s , (b) DC bus voltages V_{C_1} and V_{C_2} , and (c) output voltage V_o and current I_o .

**FIGURE 4.21**

Operation under stored-energy operation mode for unbalanced nonlinear load. (a) Battery current I_{bat} , (b) DC bus voltage V_{c1} , (c) DC bus voltage V_{c2} , and (d) output voltage V_o and current I_o .


FIGURE 4.22

Proposed new single-phase to two-phase on-line UPS system with reduced number of switches.


FIGURE 4.23

Control strategy for the DC/AC inverter.

same as those described in Section 4.2. The difference lies in the back-end inverter, where one more leg is added for the second phase, together with the corresponding low-pass LC filter.

A diagram of the implemented SPWM control strategy for the DC/AC inverter is shown in Figure 4.23. The control strategy is similar to that used

for the single-phase UPS system from Section 4.2. It uses two control loops: one outer voltage loop and one inner current loop. The outer voltage control loop is slow and is in charge of tracking the steady-state output voltage. The inner current control loop is much faster and improves the dynamic response of the inverter. The reference-modulating signals for the two inverter legs are phase shifted 120° from each other.

4.2.2.2 Simulation Results

Figure 4.24 shows the simulation results for the output line voltage V_{ab} and the load current I_{ab} in normal operating mode feeding a standard nonlinear load.

Figure 4.25 shows output phase voltages V_a and V_b , as well as output load currents I_a and I_b for a nonsymmetrical resistive load: $P_a=500$ W and $P_b=350$ W. The output voltages are high-quality sine waves, with THD less than 5%.

Figure 4.26 shows output phase voltages V_a and V_b , as well as output load currents: I_a for a standard rectifier ($P_a=350$ W) and I_b for a resistive load ($P_b=350$ W). The output voltages are high-quality sine waves, with THD less than 1%.

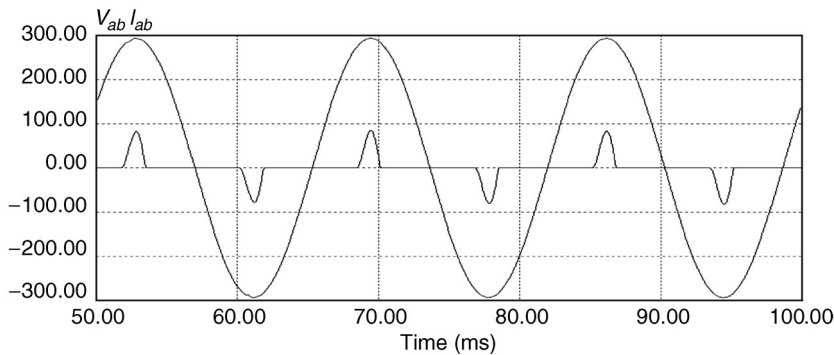


FIGURE 4.24

Output line voltage V_{ab} and load current I_{ab} .

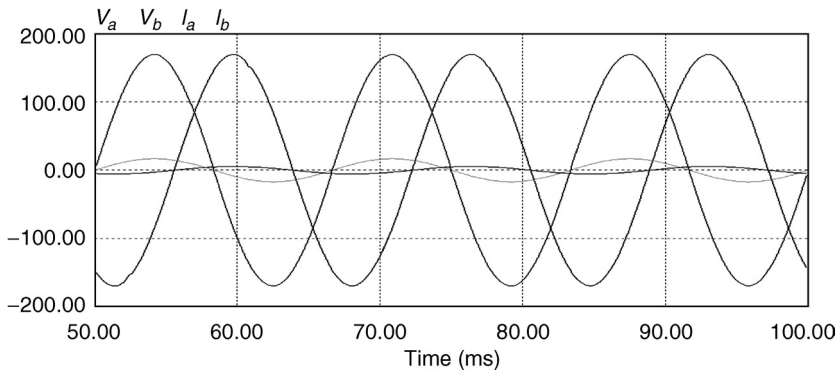
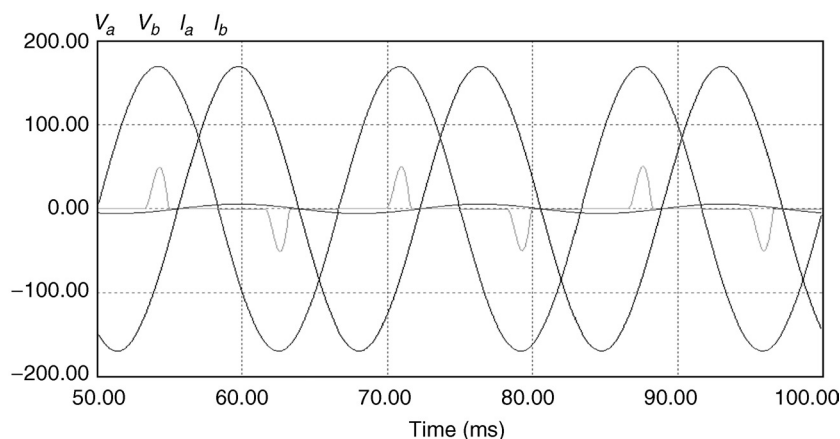


FIGURE 4.25

Output phase voltages V_a and V_b , and load currents I_a and I_b for a nonsymmetrical resistive load.

**FIGURE 4.26**

Output phase voltages V_a and V_b , and load currents I_a and I_b .

Figure 4.27 shows the dynamic performance of the proposed UPS system with a step-changing load. As can be seen from the simulation results, the dynamic performance of the proposed UPS system is excellent. The UPS system is very stable and there have not been any distortions observed in the output voltages during the transition from no load to half load, and finally to full load.

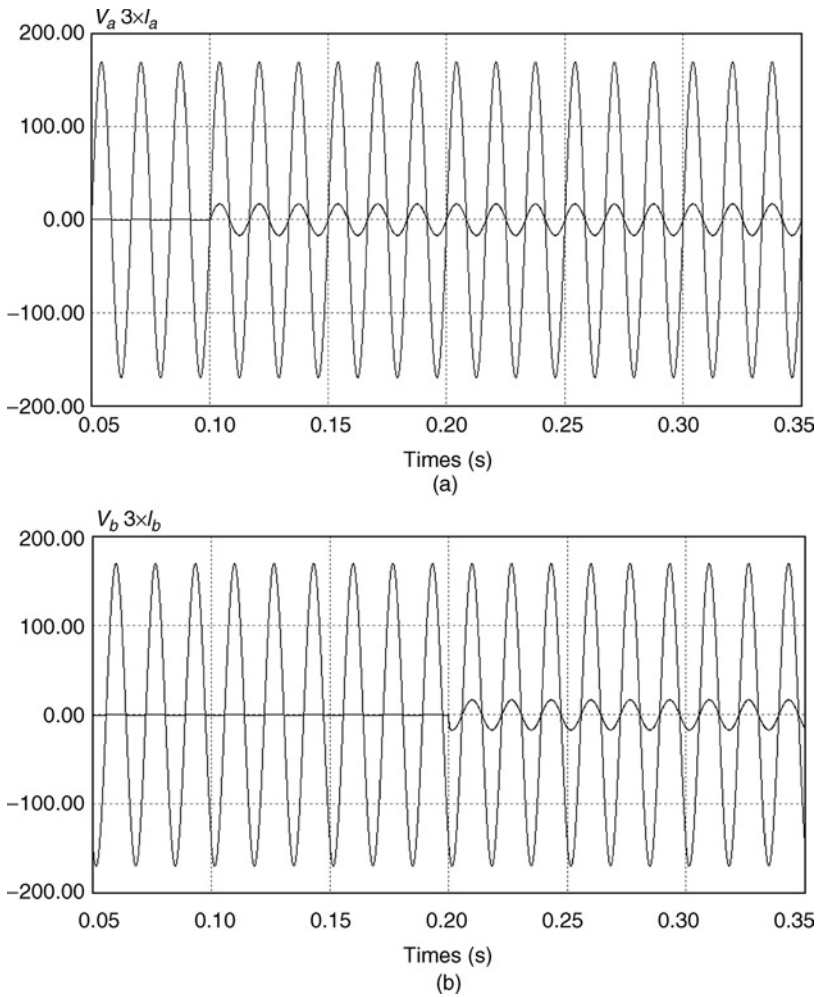
4.2.3 Single-Phase to Three-Phase On-Line UPS System

A new single-phase to three-phase UPS system is derived from the UPS system described in Section 4.3 by adding one more leg to the back-end DC/AC inverter. The proposed UPS system is shown in Figure 4.28.

4.2.3.1 Basic Principles of Operation

The operating principles regarding the front-end AC/DC rectifier, the DC/DC step-down converter, and the DC/DC step-up converter are the same as those described in Section 4.3. The difference lies in the back-end inverter, where one more leg has been added for the third phase, together with the corresponding low-pass LC filter.

The control strategy is similar to that used for the single-phase UPS system from Section 4.3. It uses two control loops: one outer voltage loop and one inner current loop. The outer voltage control loop is slow and is in charge of tracking the steady-state output voltage. The inner current control loop is much faster and improves the dynamic response of the inverter. The reference-modulating signals for the three inverter legs are phase shifted 120° from each other.

**FIGURE 4.27**

Output phase voltages V_a and V_b , and load currents I_a and I_b for step-changing loads. (a) Output phase voltage V_a and current I_a , and (b) output phase voltage V_b and current I_b .

4.2.3.2 Simulation Results

Figure 4.29 shows the output phase voltages V_a , V_b , and V_c as well as the output load currents I_a , I_b , and I_c for a nonsymmetrical resistive load: $R_a=50\ \Omega$, $R_b=25\ \Omega$, and $R_c=100\ \Omega$. The output voltages are high-quality sine waves with THD less than 5%.

Figure 4.30 shows the simulation results for the output line voltages V_{ab} , V_{bc} , and V_{ca} , and for the load currents I_{ab} , I_{bc} , and I_{ac} with a nonsymmetrical three-phase load.

Finally, Figure 4.31 shows the dynamic performance of the proposed UPS system with step-changing loads. A standard rectifier load has been

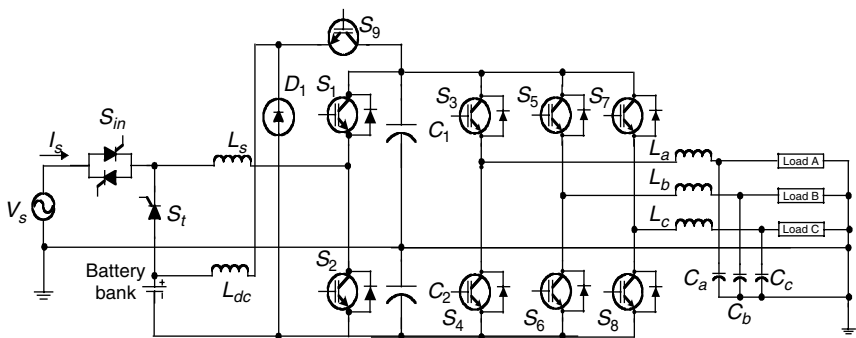


FIGURE 4.28
Proposed new single-phase to three-phase on-line UPS system with reduced number of switches.

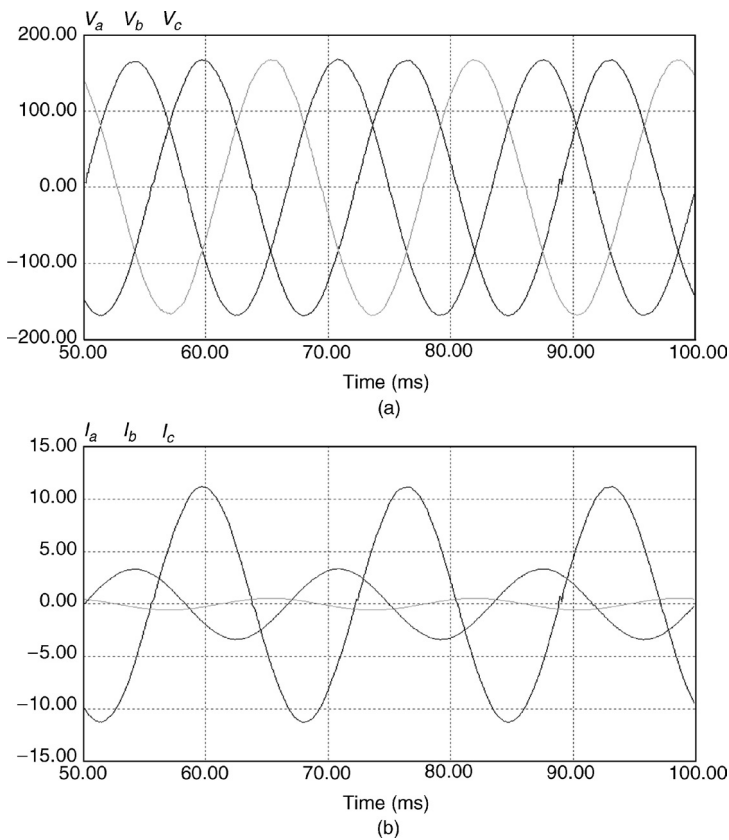
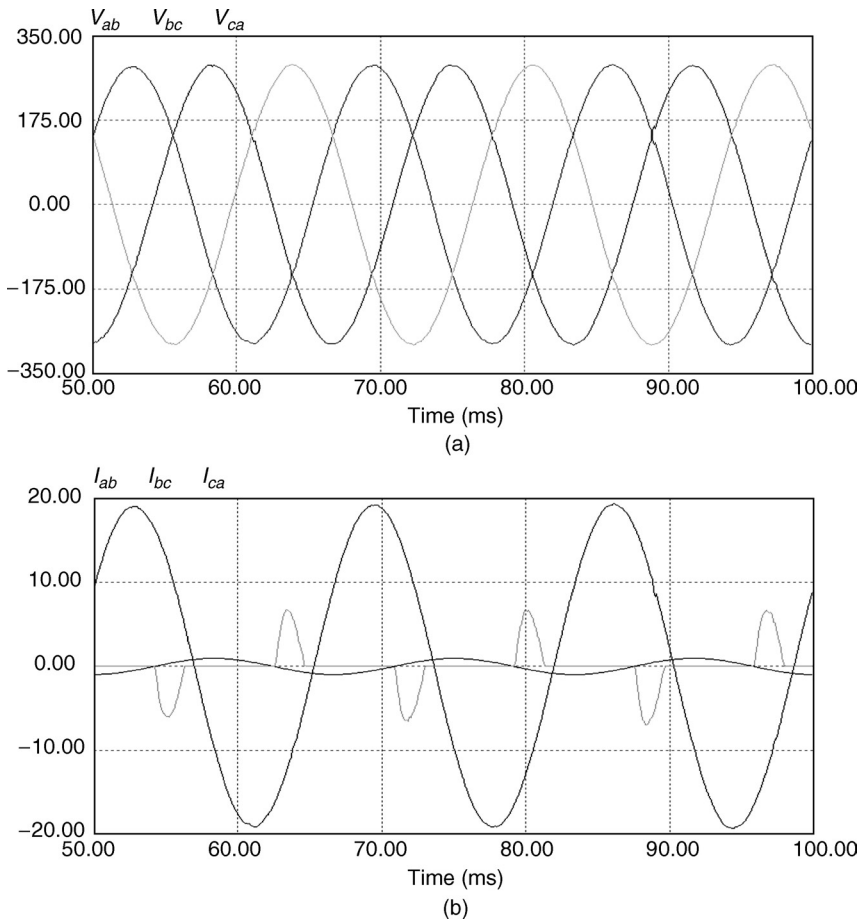


FIGURE 4.29
Simulation results for output phase voltages V_a , V_b , and V_c and for load currents I_a , I_b , and I_c . (a) Output phase voltages V_a , V_b , and V_c , and (b) phase currents I_a , I_b , and I_c .

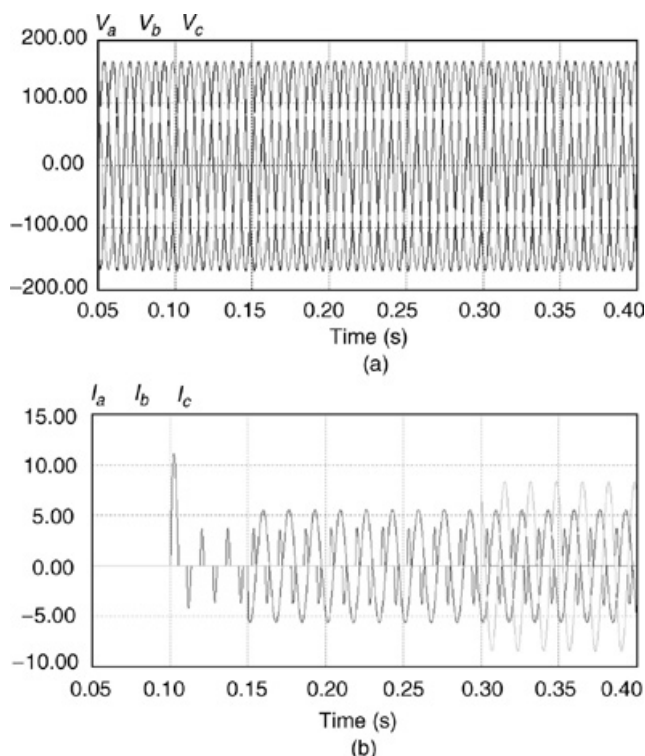
**FIGURE 4.30**

Simulation results for output line voltages V_{ab} , V_{bc} , and V_{ca} , and for load currents I_{ab} , I_{bc} , and I_{ca} . (a) Output line voltages V_{ab} , V_{bc} , and V_{ca} , and (b) line currents I_{ab} , I_{bc} , and I_{ca} .

connected in phase A at 0.1 s, followed by a resistive load $R_b=30\ \Omega$ in phase B after 0.05 s, and finally by another resistive load $R_c=20\ \Omega$ after 0.15 s. As can be seen from the simulation results, the dynamic performance of the proposed UPS system is excellent. The UPS system is very stable, and no distortions in the output voltages have been observed.

4.2.4 Performance Analyses and Cost Evaluation

The performance of a UPS system is evaluated in terms of several factors. The first and the most important factor is the quality of the output voltage, which should be sinusoidal with a low THD. The typical requirement is THD less than 5%. As can be seen from the experimental results, the quality of the output voltage in all the proposed three UPS systems is excellent. Not only is the

**FIGURE 4.31**

Output phase voltages V_a , V_b and V_c , and phase currents I_a , I_b and I_c for step-changing loads. (a) Output phase voltages V_a , V_b , and V_c , and (b) phase currents I_a , I_b , and I_c .

THD of the output voltage below 5% with linear loads but also, due to the multiple control loop strategies used, the THD is very low even with highly nonlinear loads. This is a performance feature characteristic only of state-of-the-art UPS systems. Generic UPS systems usually specify the THD of the output voltage to be less than 5% only with linear loads.

The multiple control loop strategies also significantly improve the dynamic performance of the proposed UPS systems, resulting in a very good transient response to input voltage disturbances and step-changes in the load. As shown by the results, there are no distortions in the output voltages due to the step-change in the load or disturbances in the input voltage.

The excellent stability of the proposed systems has been verified by numerous simulations and experiments, where many different operating conditions have been tested, including input voltage sags and brownouts, input voltage blackouts, step-changes in the load from 0 to 50% and after that to 100%, and transition from the normal to the stored-energy mode of operation.

An important factor in terms of evaluating the performance of UPS systems is also the power factor (PF) of the input current. It is highly desirable that the power factors be high in order to meet the corresponding standards and to

better utilize the whole system. A high power factor means a high displacement factor (DF) and low THD of the input current. The simulation and experimental results show excellent PF correction capabilities of the half-bridge front-end rectifier. The DF is unity and the THD of the input current is very low.

The next factor for evaluating the performance of UPS systems is the transfer time between the normal operating mode and stored-energy operating mode. In terms of this aspect, the on-line UPS topology is superior. Its configuration naturally ensures that the load is continuously supplied with power without any transfer time. Experimental results from Figure 4.28 confirm that the proposed UPS systems have essentially zero transfer time as any truly double-conversion topology.

An important performance feature of UPS systems is its reliability. The weakest point in any UPS system is the battery. It is well documented that 92% of all UPS failures are due to battery malfunction. This weakness comes from the very nature of the electrochemical battery and there is not much that a power electronics design engineer can do about it. Nevertheless, when designing a state-of-the-art UPS system, it is imperative to provide the best operating conditions possible for the battery bank in order to prolong the life of the battery and increase its reliability. In this sense, connecting the battery directly to the high-voltage DC-link bus is not the best option because this voltage is not very tightly regulated and can experience quite large ripples at low input voltages and maximum load. In contrast, when using a low-voltage battery bank interfaced with a battery charger, as shown in the proposed UPS systems, the battery is provided with a tightly regulated charging voltage. In fact, the batteries are normally in the float mode with no bus ripple across them. This prolongs the battery life and decreases the chances of battery failure, increasing the overall reliability of the whole UPS system.

Another point worth mentioning is that the double-conversion nature of the proposed UPS systems allows continuous power conditioning during sags and brownouts without battery involvement in frequent charge/discharge cycles, which further protects the battery's state of health.

The next important point when evaluating the reliability of a UPS system is the power electronics circuitry. The simpler the power circuits, the higher the reliability. Experience shows that semiconductor components are most prone to failures compared to passive components. In this sense, the smaller the number of semiconductors, the higher the reliability as

$$MTBF_{total} = \frac{1}{\frac{1}{MTBF_1} + \frac{1}{MTBF_2} + \frac{1}{MTBF_3} + \cdots + \frac{1}{MTBF_i}} \quad (4.23)$$

where $MTBF_{total}$ is the mean time between failure for the whole UPS system and $MTBF_i$ is the mean time between failure for the i th component.

In all three proposed UPS systems, one of the IGBTs in the conventional bidirectional buck-boost converter has been eliminated, which results in a higher reliability.

TABLE 4.1

Cost comparison between the proposed single-phase UPS system and its conventional counterpart

Component	Proposed UPS system (Fig. 4.4)				Conventional UPS system (Fig. 4.3)			
	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)
IGBT	S_1-S_4	4	35.00	140.00	S_1-S_6	6	35.00	210.00
	S_5	1	2.22	2.22	—	—	—	0
Diode	D_1	1	1.78	1.78	—	—	—	0
SCR	S_t	1	3.20	3.20	—	—	—	0
Static switch	S_{in}	1	6.40	6.40	S_{in}	1	6.40	6.40
	Bypass	1	6.40	6.40	Bypass	1	6.40	6.40
Inductors	L_s	1	26.00	26.00	L_s	1	26.00	26.00
	L_{dc}	1	8.21	8.21	L_{dc}	1	70.22	70.22
	L_o	1	5.25	5.25	L_o	1	5.25	5.25
Capacitors	C_1, C_2	2	18.30	36.60	C_1, C_2	2	18.30	36.60
Miscellaneous		1	50.00	50.00		1	50.00	50.00
Total cost				286.06				410.87
Total savings				124.81				−124.81

Apart from the excellent performance characteristics, the proposed UPS systems are less expensive than their conventional counterparts, due to the elimination of the output transformer and the battery step-up DC/DC converter.

The low-frequency isolation transformer is the bulkiest, heaviest, and most expensive component in a typical UPS system. A typical 1 kVA 60 Hz isolation transformer costs about \$150 and weighs about 15 lbs.

The elimination of the step-up DC/DC converter not only saves one active switch but also relaxes the current's requirements for the inductor L_{dc} in the battery charger, which, as can be seen from Table 4.1, has the largest cost factor. The overall cost savings for the proposed single-phase on-line UPS system from Figure 4.4 is \$124.81 or more than 30% compared to its conventional counterpart from Figure 4.3. In an extremely competitive market, such as the low- to middle-power class UPS systems, the cost is of particular high importance.

4.2.5 Conclusions

The proposed UPS systems based on half-bridge converters have many desirable features. First, they have excellent performance characteristics including:

- High-quality sinusoidal output voltages, even with nonlinear loads.
- Unity input power factor.
- Excellent transient characteristics and stability.
- Zero transfer time between the normal mode and the stored-energy mode of operation.

- Excellent power-conditioning throughout a wide input voltage variation range in both amplitude and frequency.
- Small weight, size, and cost.

By making use of the fact that the front-end rectifier is of a boost type, the boost converter in the conventional UPS system from Figure 4.3 has been eliminated, resulting in a substantial cost, weight, and size savings without any compromise in the performance. The smaller number of components also increases the overall reliability of the UPS systems.

In sum, the proposed UPS systems with their compactness, low cost, and excellent performance are strong candidates for optimal low-cost UPS systems for low-power applications, such as personal computers (PCs). It should be mentioned, however, that in the case of the unbalanced load, when the current drawn during the positive half cycle is not equal to the current drawn during the negative half-cycle, the performance of the UPS systems, based on half-bridge converters, is compromised during the stored-energy mode of operation. Since the battery bank charges the two capacitors at a time, the unbalance in the DC voltages V_{C_1} and V_{C_2} cannot be compensated. As a result, the output voltage can be distorted. An example of such a distortion is shown in Figure 4.21, where the UPS system supplies an unbalanced load. This drawback can be eliminated by using a novel AC/DC rectifier at the front-end of the UPS system, as proposed in Section 4.3. The new AC/DC rectifier can not only compensate for any unbalances in the DC-link capacitor voltages but also has two times lower voltage stresses across the active switches compared to the conventional half-bridge rectifier, which results in a direct increase in the overall efficiency and reliability of the whole system. Three new UPS systems based on the novel AC/DC rectifier are proposed in Section 4.3.

4.3 New On-Line UPS Systems Based on a Novel AC/DC Rectifier

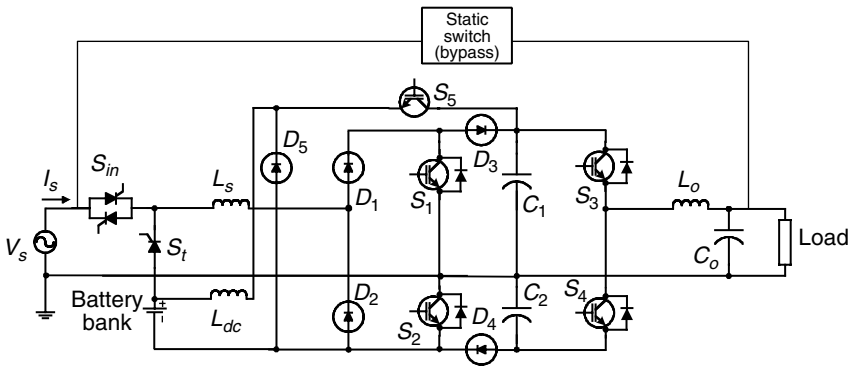
Three new reduced-parts on-line UPS system, based on a novel integrated rectifier/boost converter, are presented in this section. A comprehensive explanation of their principles of operation is given, along with the results of extensive computer simulations.

4.3.1 Reduced-Parts Single-Phase On-Line UPS System

The new on-line single-phase UPS system, based on a novel AC/DC rectifier, is shown in Figure 4.32.

4.3.1.1 System Description

The UPS system shown in Figure 4.32 has a front-end AC/DC rectifier with PFC capabilities, a DC/AC inverter, a step-down DC/DC converter, a

**FIGURE 4.32**

Proposed single-phase UPS system with novel AC/DC rectifier.

battery bank, an input switch S_{in} , a transfer switch S_t in the form of a thyristor, and a bypass static switch.

The AC/DC rectifier consists of an input inductor L_s , switches S_1 and S_2 , diodes D_1, D_2, D_3 and D_4 , and two capacitors C_1 and C_2 . The DC/AC inverter consists of a split DC bus, switches S_3 and S_4 , and an output LC filter. It operates in a high-frequency SPWM pattern in order to provide a high-quality sinusoidal output voltage. The step-down DC/DC converter consists of switch S_5 , diode D_5 , and DC inductor L_{dc} . Its purpose is to step down the high DC bus voltage to the low DC battery voltage, thus controlling the charge of the battery bank.

The input switch S_{in} disconnects the UPS system from the grid when the UPS system is in the stored-energy mode of operation in order to prevent back feeding of power from the battery bank to the grid. The transfer switch S_t is used to transfer the input power source from the AC line to the battery. The bypass static switch is used to “bypass” the UPS system in case of failure or if maintenance is required.

4.3.1.2 Basic Principles of Operation

The proposed UPS system has three operating modes: normal mode, stored-energy mode, and bypass mode. In the normal mode of operation, the input voltage is present and it is within the permissible tolerance range. Since the proposed UPS system is essentially a double-conversion type, power is converted from AC to DC by the AC/DC rectifier and passed to the DC/AC inverter, which in turn converts it from DC to AC and supplies the load continuously with a high-quality AC power. The transfer switch S_t is off.

During the normal mode of operation, the front-end converter has three functions: to rectify the input AC voltage into DC, to boost the DC voltage to a level required for proper operation of the back-end inverter, and to keep the power factor close to unity. Switch S_1 is used for current shaping and voltage boosting during the positive half-period of the input AC voltage. By

closing and opening S_1 , the current through inductor L_s is forced to follow a sinusoidal reference, which is in phase with the input AC voltage. In this way, the power factor is kept close to unity. At the same time, it maintains a constant DC bus voltage across capacitor C_1 . When switch S_1 is turned on at positive V_s , the voltage across the input inductor L_s is

$$V_{L_s} = L_s \frac{di_s}{dt} = V_s \quad (4.24)$$

The voltage across the input inductor is positive and the input current increases. During this time, diode D_3 prevents capacitor C_1 from discharging. The corresponding circuit is shown in Figure 4.33.

When S_1 is turned off, the stored energy in L_s is transferred to C_1 . The expression for the voltage across the input inductor L_s is

$$V_{L_s} = L_s \frac{di_s}{dt} = V_s - V_{C_1} \quad (4.25)$$

Since $V_{C_1} > V_s$, the voltage across the input inductor is negative and the input current decreases. The corresponding circuit is shown in Figure 4.34.

The same strategy is used for charging the bottom capacitor C_2 during the negative half-period of the input AC voltage, but with S_2 active. When switch S_2 is turned on at negative V_s , the voltage across the input inductor L_s is

$$V_{L_s} = L_s \frac{di_s}{dt} = -V_s \quad (4.26)$$

The voltage across the input inductor is negative and the input current decreases. During this time, diode D_4 prevents capacitor C_2 from discharging. The corresponding circuit is shown in Figure 4.35.

When switch S_2 is turned off, the stored energy in L_s is transferred to capacitor C_2 . The expression for the voltage across the input inductor L_s is

$$V_{L_s} = L_s \frac{di_s}{dt} = -V_s + V_{C_2} \quad (4.27)$$

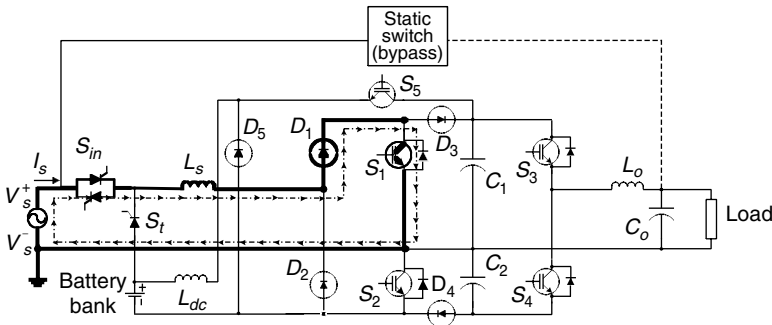
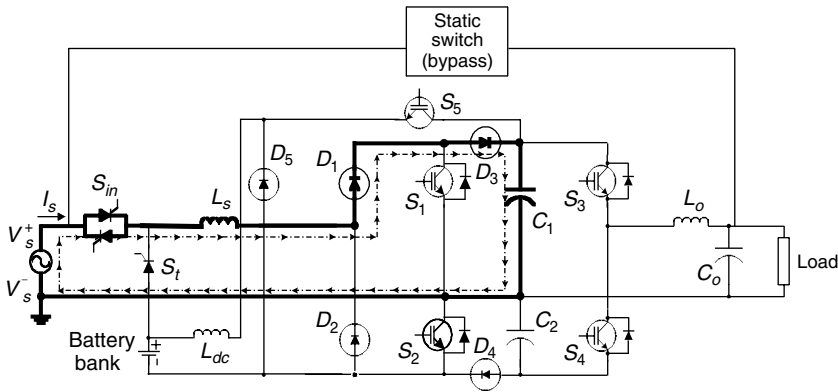
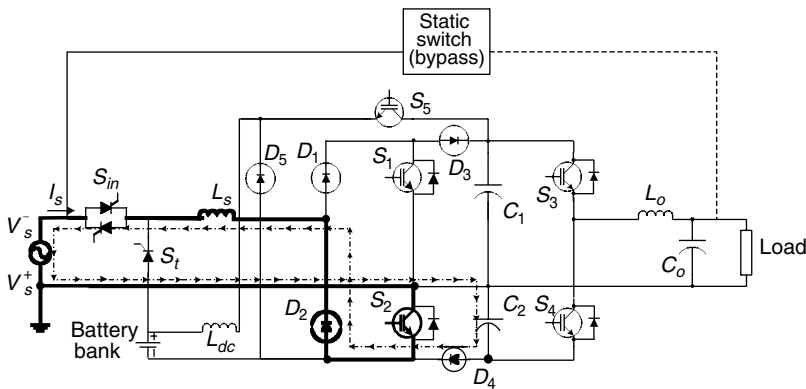


FIGURE 4.33

Corresponding circuit diagram for the positive half-cycle of the input voltage with S_1 closed.

**FIGURE 4.34**

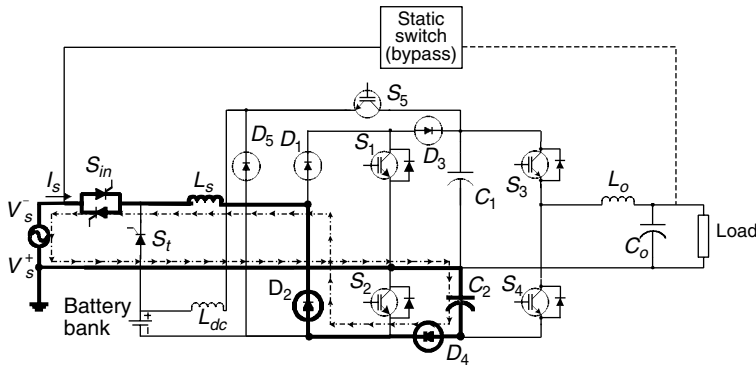
Corresponding circuit diagram for the positive half-cycle of the input voltage with S_1 open.

**FIGURE 4.35**

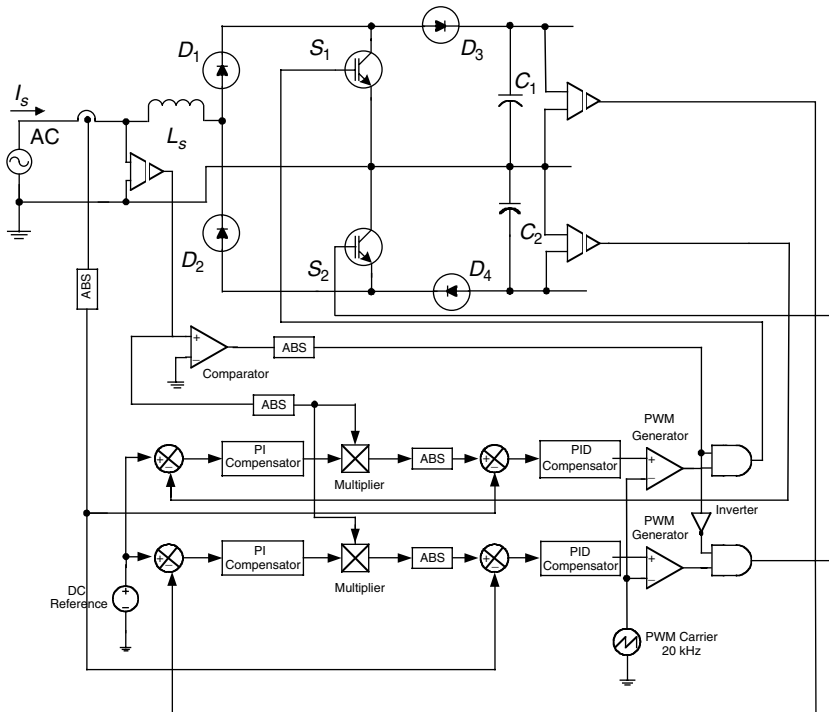
Corresponding circuit diagram for the negative half-cycle of the input voltage with S_2 closed.

Since $V_{C_2} > V_s$, the voltage across the input inductor is positive and the input current increases. The corresponding circuit is shown in [Figure 4.36](#).

A diagram of the implemented control is shown in [Figure 4.37](#). The control strategy for the AC/DC rectifier uses multiple control loops for each switch: one outer voltage loop and one inner current loop. The outer control loop uses the voltage of the output DC-link capacitor as a feedback signal, which is compared with a reference signal. A *PI* integrator compensates the error. The output of the *PI* integrator is used as a reference signal for the inner current regulator loop, which uses the input inductor current as a feedback signal. The minor current loop is fast and gives good dynamic response, resulting in a very good input power factor. The outer voltage loop is slower and keeps the output DC-link voltage stable at 480 V: 240 V for each capacitor C_1 and C_2 . The switching frequency is 20 kHz.

**FIGURE 4.36**

Corresponding circuit diagram for the negative half-cycle of the input voltage with S_2 open.

**FIGURE 4.37**

Control strategy for the AC/DC rectifier.

The battery charger is a buck-type DC/DC converter, which steps down the high DC-link voltage from 480 V to a low floating battery voltage of 58 V. It operates in the following way. When switch S_5 is turned on, the voltage across inductor L_{dc} is positive.

$$V_{L_{dc}} = V_{dc} - V_{bat} \quad (4.28)$$

During the positive half-cycle, when switch S_5 is turned on, the voltage across inductor L_{dc} is positive and the inductor current starts increasing, following the current path: $V_{C_1}^+ - S_5 - L_{dc} - V_{bat}^-$ —reverse diode of $S_2 - V_{C_1}^-$ and charging the battery. When switch S_5 is turned off, the inductor current circulates in the current path $V_{bat}^- - D_5 - L_{dc} - V_{bat}^+$.

During the negative half-cycle, when switch S_5 is turned on, the current path is: $V_{C_1}^+ - S_5 - L_{dc} - V_{bat}^- - D_2 - L_s - V_s - V_{C_1}^-$. In this way, the high DC capacitor voltage V_{C_1} is stepped down to low battery voltage V_{bat} by switching switch S_5 on and off.

$$V_{bat} = D \times V_{C_1} \quad (4.29)$$

Figure 4.38 shows the voltage across diode D_5 , the current through inductor L_{dc} , and the output voltage V_{out} across the battery terminals [12].

The DC/AC inverter is a typical half-bridge inverter. Its operation has been explained in Section 2.10.2.

When the input AC voltage is beyond the permissible tolerance range, the UPS system works in the stored-energy mode of operation. Switch S_{in} is turned off and switch S_i is turned on, transferring the input from the AC line to the battery bank. The low battery voltage of 48 V needs to be boosted to a high DC voltage of 480 V for proper operation of the back-end inverter.

In this mode of operation, the AC/DC rectifier works like a DC/DC boost converter in the following manner. When switches S_1 and S_2 are turned on, the low input battery voltage is applied across the inductor L_s and the inductor current starts increasing. The current path is: $V_{bat}^+ - L_s - D_1 - S_1 - S_2 - V_{bat}^-$. When transistor S_1 is turned off, the current path is changed to: $V_{bat}^+ - L_s - D_1 - D_3 - C_1 - S_2 - V_{bat}^-$ and the upper capacitor is charged.

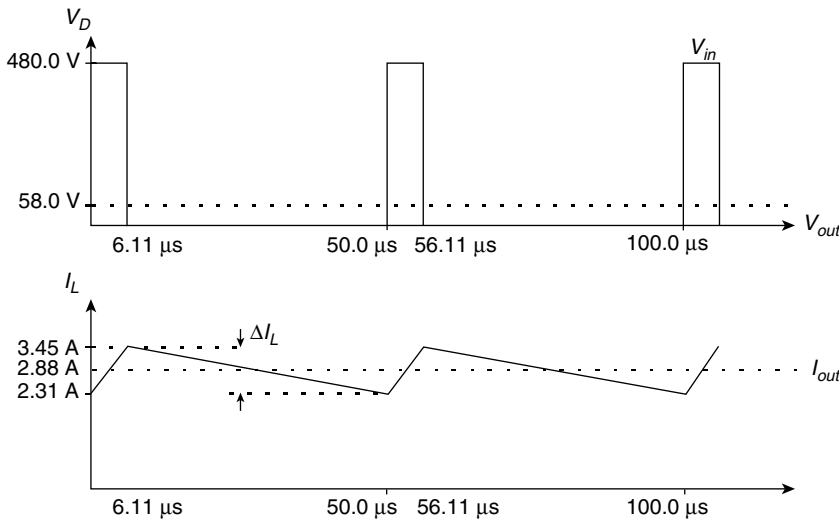


FIGURE 4.38

Operation of the DC/DC step-down converter.

Accordingly, when transistor S_2 is turned off the current path is: $V_{bat}^+ - L_s - D_1 - S_1 - C_2 - D_4 - V_{bat}^-$ and the bottom capacitor is charged. In this way, the duty ratio of transistor S_1 controls the voltage of the upper capacitor C_1 and the duty ratio of transistor S_2 controls the bottom capacitor C_2 . Adjusting the duty ratio of the two switches can compensate any unbalance between the two capacitor's voltages, which can occur when the load draws more current during one-half of the 60 Hz cycle than during the other half-cycle. This situation is unavoidable during the start-up of loads that have uncontrolled AC/DC rectifiers with large DC capacitors as part of their power supply. Conventional boost converters that are commonly used to step up the low battery voltage charge both capacitors C_1 and C_2 at the same time and are incapable of compensating any difference between the voltages V_{C_1} and V_{C_2} once it occurs. As a result, the output voltage from the back-end DC/AC inverter can be compromised as shown in [Figure 4.21](#).

4.3.1.3 Simulation Results

Extensive computer simulations have been carried out, using PSIM simulation software, to help design the control for the new UPS system. The system parameters have been chosen as follows:

- Input voltage: single-phase 120 VAC $\pm 25\%$
- Battery voltage: 48 V
- DC-link bus voltage: 480 V (2×240 V)
- Output voltage: 120 VAC $\pm 5\%$
- Output frequency: 60 Hz $\pm 0.5\%$
- THD: $< 5\%$
- Output power: 1 kVA continuous
- Switching frequency: 20 kHz

After careful design considerations, described in Section 4.2.1.3, regarding the input current PF and THD, DC-link voltage ripples, and cut-off frequency of the output low-pass filter, the following values for the passive components have been chosen:

- $L_s = 350 \mu\text{H}$
- $L_{dc} = 2.22 \text{ mH}$
- $L_o = 100 \mu\text{H}$
- $C_o = 20 \mu\text{F}$
- $C_1 = 4700 \mu\text{F}$
- $C_2 = 4700 \mu\text{F}$

The input AC voltage V_s and current I_s are shown in [Figure 4.39](#). The input power factor is in effect equal to unity.

Currents through the IGBTs S_1 and S_2 are shown in [Figure 4.40](#). As it is clear from the figure, switch S_1 is active during the positive half-cycle of the input voltage and switch S_2 is active during the negative half-cycle of the input voltage.

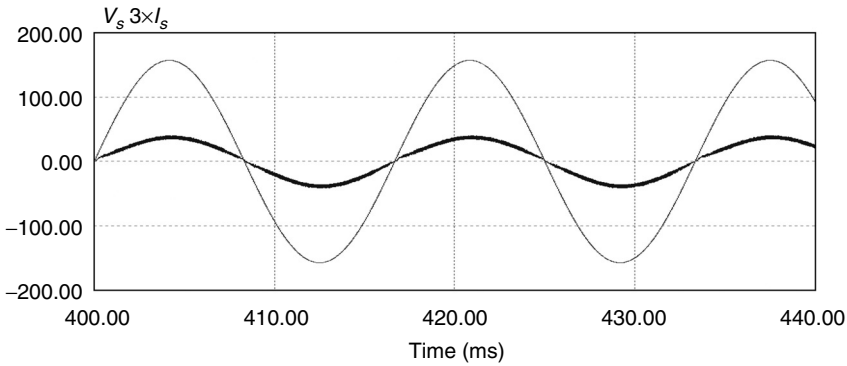


FIGURE 4.39
Input current I_s and voltage V_s .

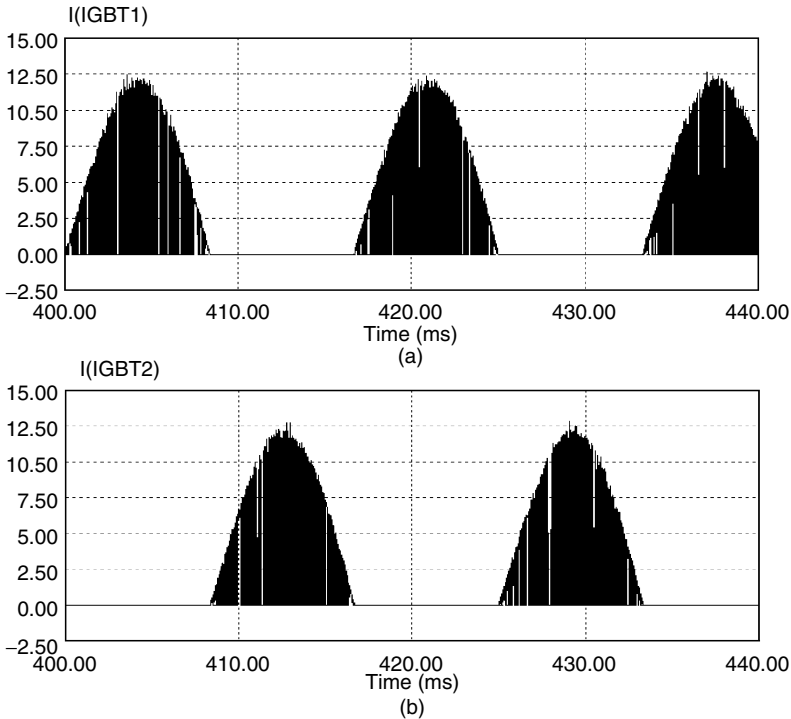


FIGURE 4.40
Currents through IGBTs S_1 and S_2 . (a) Current through IGBT S_1 , and (b) current through IGBT S_2 .

Figure 4.41 shows the regulation of the DC-link bus voltages across capacitors C_1 and C_2 for a balanced nonlinear load.

Figure 4.42 shows the output voltage V_o and load current I_o for a balanced nonlinear load. The output voltage is a high-quality sine wave with THD less than 5%.

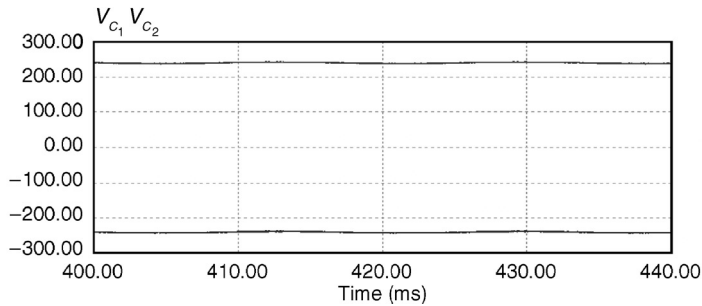


FIGURE 4.41
DC-link bus voltages for balanced nonlinear load.

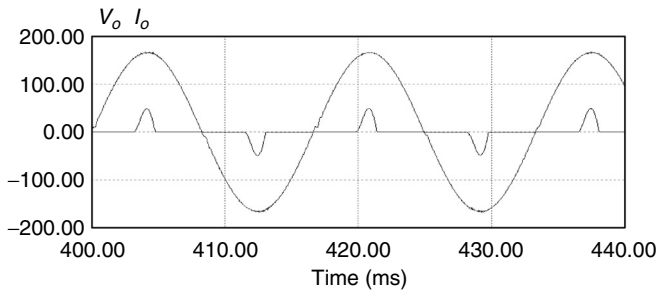


FIGURE 4.42
Output voltage V_o and current I_o for nonlinear load.

Figure 4.43 shows the dynamic performance of the proposed UPS system with step-changing loads. Initially, the system works at no load. After 0.10 s a resistive load $R=20\ \Omega$ is applied, and after another 0.10 s a standard rectifier load 350 W is connected. As can be observed from the results, the dynamic performance of the system is excellent. Deterioration of the quality of the output voltage supplied to the critical loads has not been observed. The input PF has been kept close to unity, and no stability problems have been observed.

Figure 4.44 shows the operation of the UPS system under stored-energy mode of operation for a balanced nonlinear load, when the transfer switch S_t is turned on and the input energy source is the battery bank.

Figure 4.45 shows the operation of the UPS system under stored-energy mode of operation for an unbalanced nonlinear load. The load is a half-wave rectifier. As can be seen from the simulation results, the asymmetry in the load is fully compensated thanks to the novel front-end converter, which works in this mode of operation as a boost DC/DC converter.

Figure 4.46 shows the operation of the UPS system under the normal mode of operation when the input voltage reduces from 120 to 92 V. Due to the fact that the rectifier is of a boost type, the DC-link bus voltage is maintained at 480 V without the need to switch to the battery bank. This feature extends the

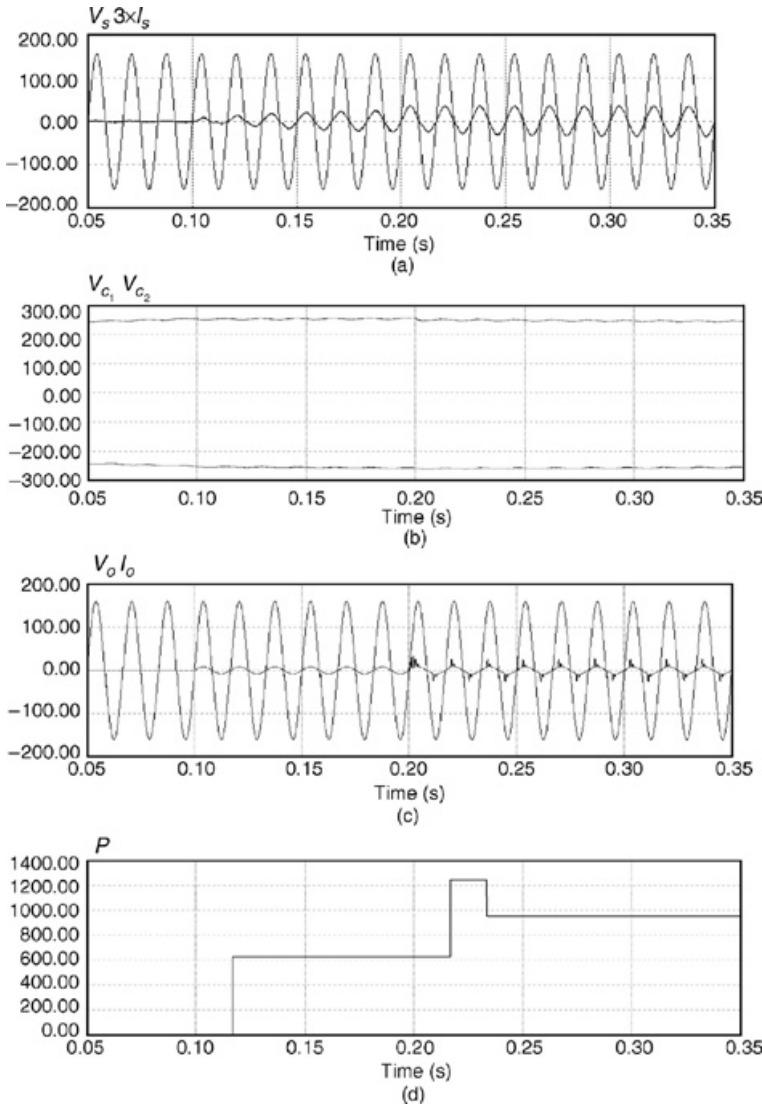
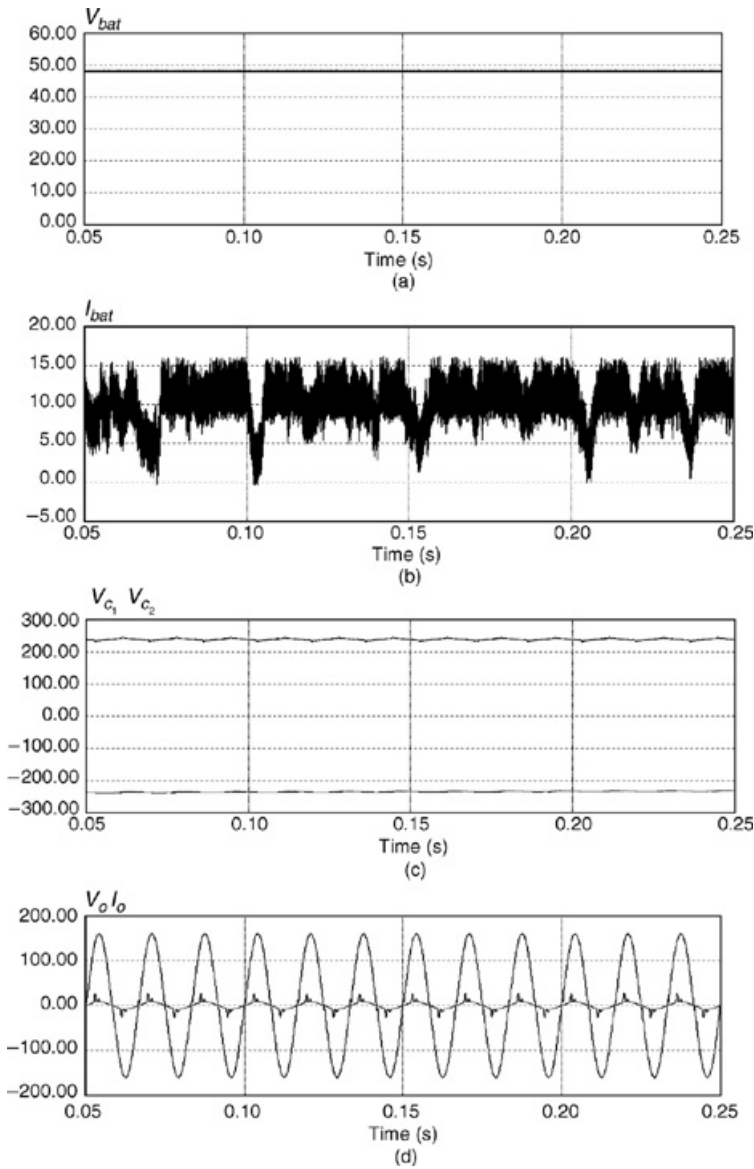


FIGURE 4.43

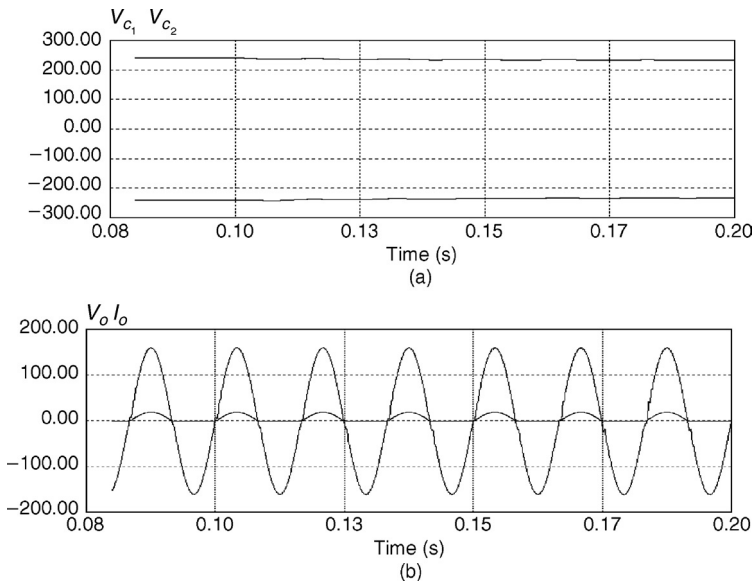
Operation under normal operation mode with step-changing loads. (a) Input voltage V_s and current I_s , (b) DC-link bus voltages V_{C1} and V_{C2} , (c) output voltage V_o and current I_o , and (d) output power P in Watts.

input voltage range at which the UPS system can work in the normal operation mode. As a result, the batteries are not forced into frequent charge/discharge cycles, which in turn extends the life of the battery, and their availability, and reliability. Parallel with the disturbance in the input, a step-change in the output load has been simulated. After 0.10 s of no load operation, a resistive load $R=40 \Omega$ is applied, and after another 0.15 s another resistive load $R=40 \Omega$

**FIGURE 4.44**

Operation under stored-energy operation mode for a balanced nonlinear load. (a) Battery voltage V_{bat} , (b) battery current I_{bat} , (c) DC-link bus voltages V_{C1} and V_{C2} , and (d) output voltage V_o and current I_o .

is connected. As can be observed from the results, the dynamic performance of the system is excellent. Deterioration of the quality of the output voltage supplied to the critical loads has not been observed. The input PF has been kept close to unity, and no stability problems have been observed.

**FIGURE 4.45**

Operation under stored-energy operation mode for an unbalanced nonlinear load. (a) DC-link bus voltages V_{C1} and V_{C2} , and (b) output voltage V_o and current I_o .

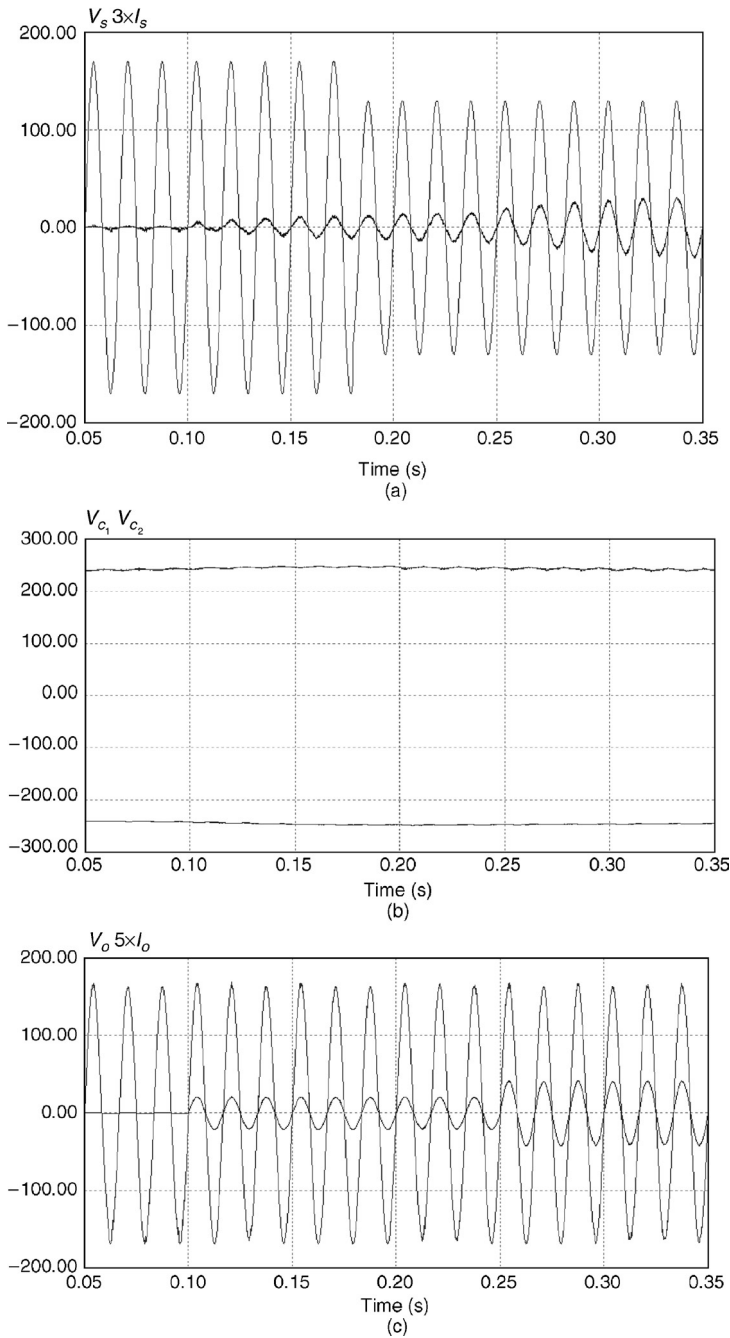
4.3.2 Single-Phase to Two-Phase On-Line UPS System

A new single-phase to two-phase UPS system is derived from the UPS system described in Section 4.3.1 by adding one more leg to the back-end DC/AC inverter. The proposed UPS system is shown in [Figure 4.47](#).

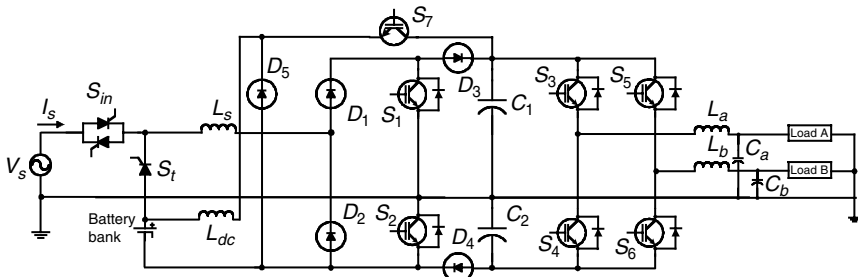
4.3.2.1 Basic Principles of Operation

The operating principles regarding the front-end AC/DC rectifier, the DC/DC step-down converter, and the DC/DC step-up converter are the same as those described in Section 4.3.1. The difference is in the back-end inverter, where one more leg is added for the second phase together with the corresponding low-pass LC filter.

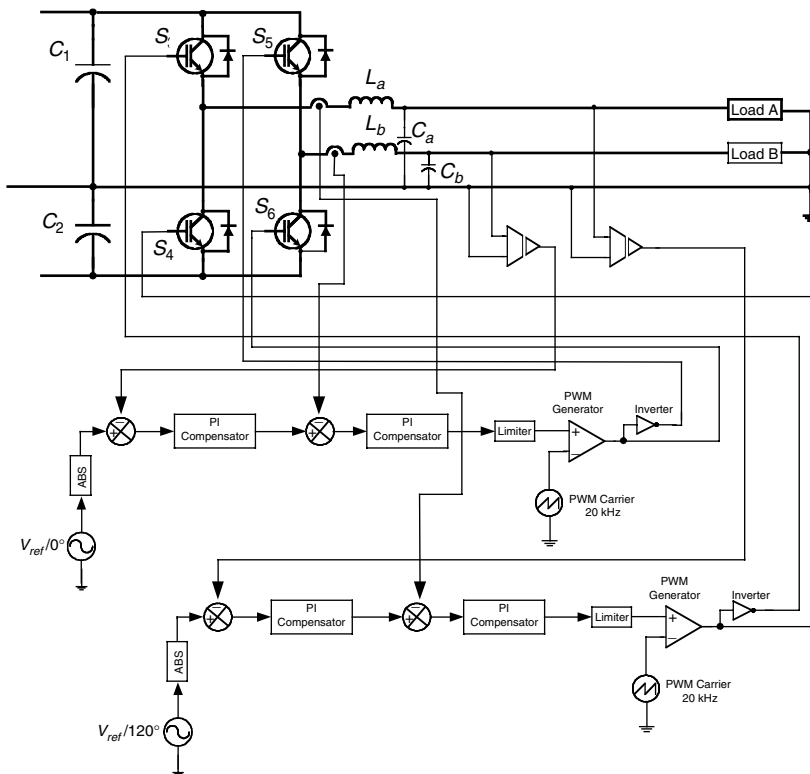
A diagram of the implemented SPWM control strategy for the DC/AC inverter is shown in [Figure 4.48](#). The control strategy is similar to that used for the single-phase UPS system from Section 4.3.1. It employs two control loops: one outer voltage loop and one inner current loop. The outer voltage control loop is slow and is in charge of regulating the output AC voltage of each phase. The inner current control loop is much faster than the outer voltage loop and improves the dynamic response of the inverter. The reference-modulating signals for the two inverter legs are phase shifted 120° from each other. The multiple control loop strategy gives a much more superior dynamic performance than the conventional single loop PID

**FIGURE 4.46**

Operation under normal mode of operation with input voltage sag from 120 to 92 V and step-changing load. (a) Input voltage V_s and current I_s , (b) DC-link bus voltages V_{C1} and V_{C2} , and (c) output voltage V_o and current I_o .


FIGURE 4.47

Proposed new single-phase to two-phase on-line UPS system with reduced number of switches.


FIGURE 4.48

Control strategy for the DC/AC inverter.

controller, whose theoretical design is much more elaborate and whose practical tuning is quite cumbersome. Multiple control loop strategies are easily achievable since modern DSP chips are optimized in such a way that multiple control algorithms can be executed at high speed, thus making it possible to achieve the required high sampling rate for a good dynamic response.

4.3.2.2 Simulation Results

Different computer simulations have been carried out, using PSIM simulation software, to help design the control for the new UPS system.

Figure 4.49 shows the output phase to neutral voltages V_a and V_b , as well as the output load currents I_a and I_b for a nonsymmetrical resistive load: $R_a=30\ \Omega$ and $R_b=60\ \Omega$. The output voltages are high-quality sine waves with a THD less than 1%.

Figure 4.50 shows the simulation results for the output line voltage V_{ab} and the load current I_{ab} in normal operating mode feeding a standard nonlinear load. Figure 4.51 shows the dynamic performance of the proposed UPS system with nonlinear step-changing loads.

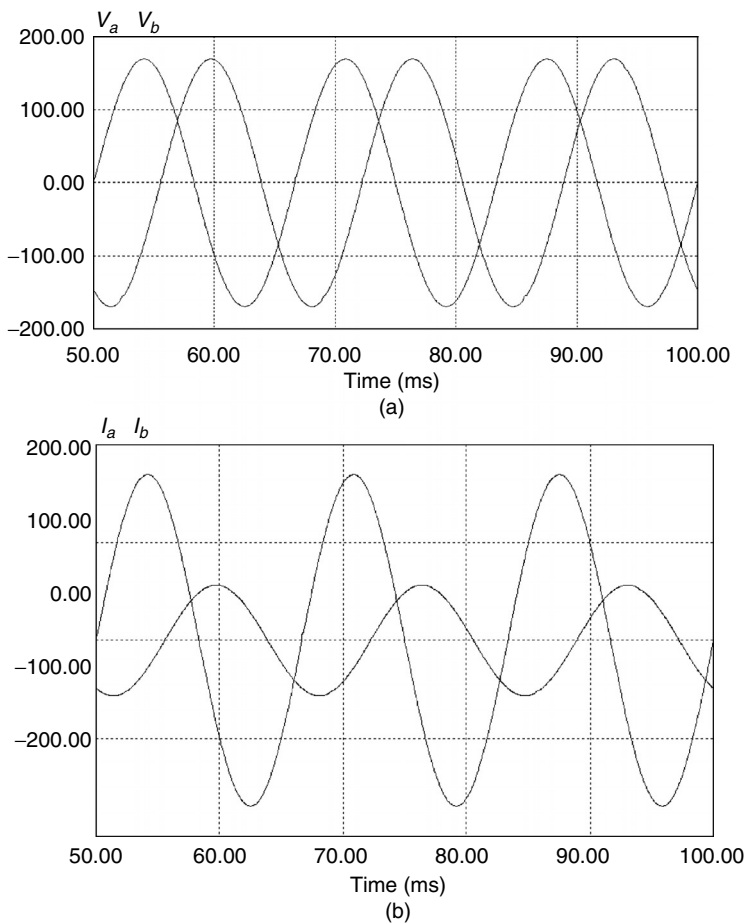


FIGURE 4.49

Output phase voltages and currents for normal operating mode. (a) Output phase voltages V_a and V_b , and (b) output phase currents I_a and I_b .

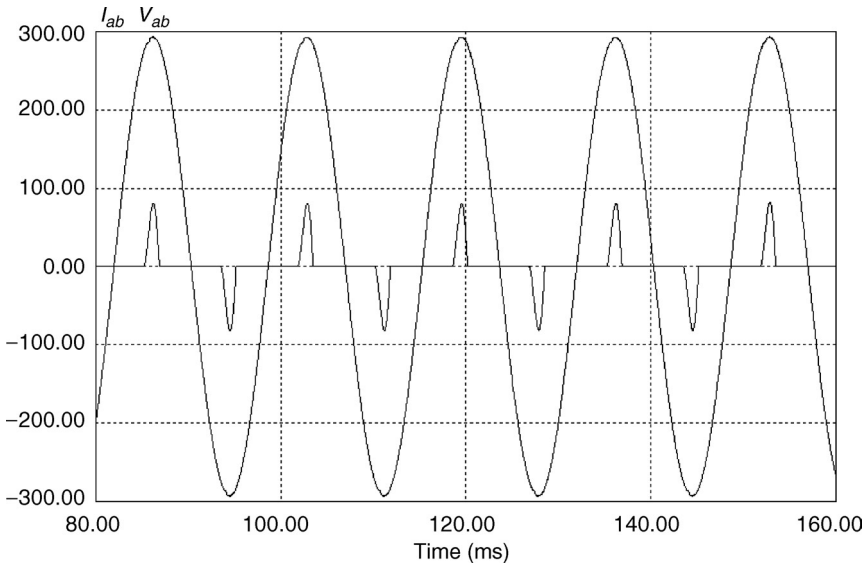


FIGURE 4.50
Output phase voltage V_{ab} and load current I_{ab} .

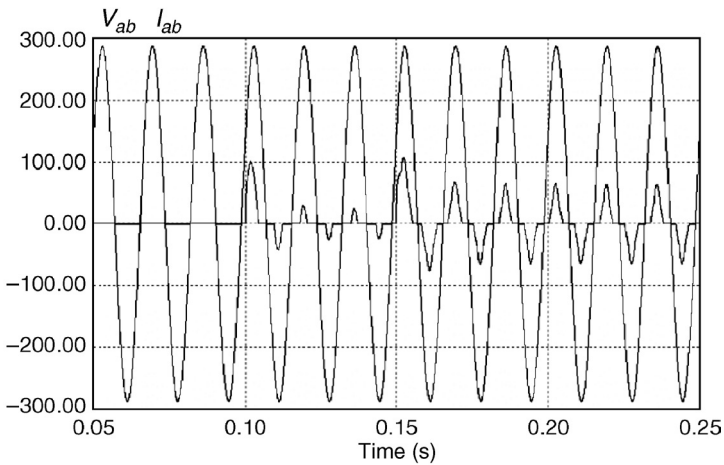


FIGURE 4.51
Output phase voltage V_{ab} and load current I_{ab} with nonlinear step-changing loads.

4.3.3 Single-Phase to Three-Phase On-Line UPS System

A new single-phase to three-phase UPS system is derived from the UPS system described in Section 4.3.1 by adding two more legs to the back-end DC/AC inverter. The proposed UPS system is shown in [Figure 4.52](#).

is not characteristic of any of the other currently known solutions for stepping up the low battery voltage in UPS systems based on half-bridge converters.

The second important benefit from the use of the novel AC/DC rectifier is that the IGBTs S_1 and S_2 are exposed to two times lower voltage stresses than those from the conventional half-bridge rectifiers. This in turn automatically yields a higher efficiency and reliability and also a potential for cost savings.

As shown in Table 4.2, the proposed single-phase UPS system from Figure 4.32 realizes a cost savings of \$113.21 or more than 27%, compared to the conventional counterpart from Figure 4.3.

4.3.5 Conclusions

The proposed UPS systems based on the novel AC/DC rectifier possess all the performance features characteristic of truly state-of-the-art UPS systems such as:

- High-quality sinusoidal output voltages even with nonlinear loads.
- Unity input power factor.
- Excellent transient characteristics and stability.
- Zero transfer time between the normal mode and the stored-energy mode of operation.

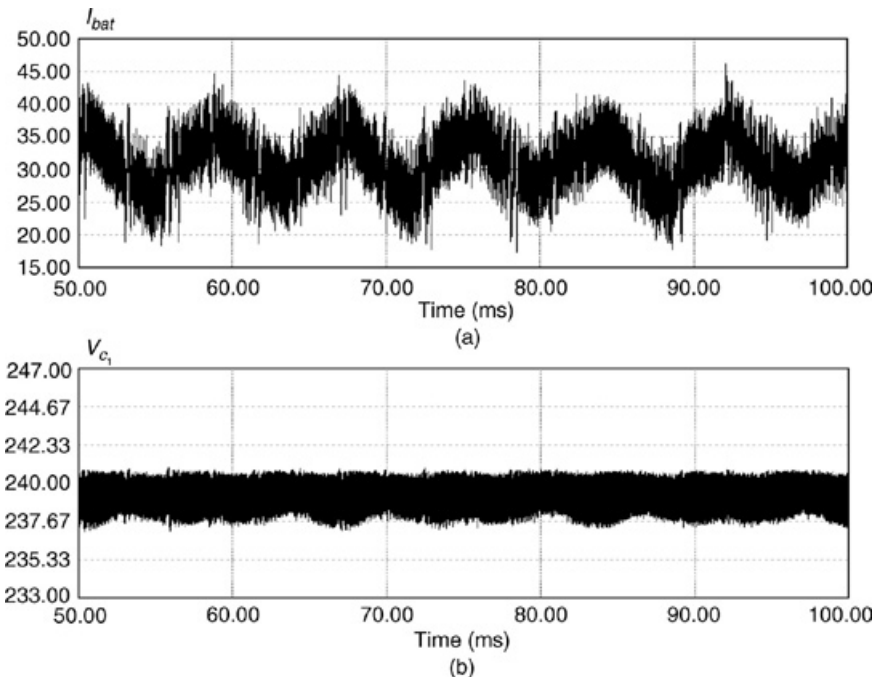


FIGURE 4.53

Simulation results for stored-energy mode of operation. (a) Battery current I_{bat} , (b) DC-link bus voltage V_{C1} , (c) DC-link bus voltage V_{C2} , (d) output phase voltages V_a , V_b , and V_c , and (e) load currents I_a , I_b , and I_c .

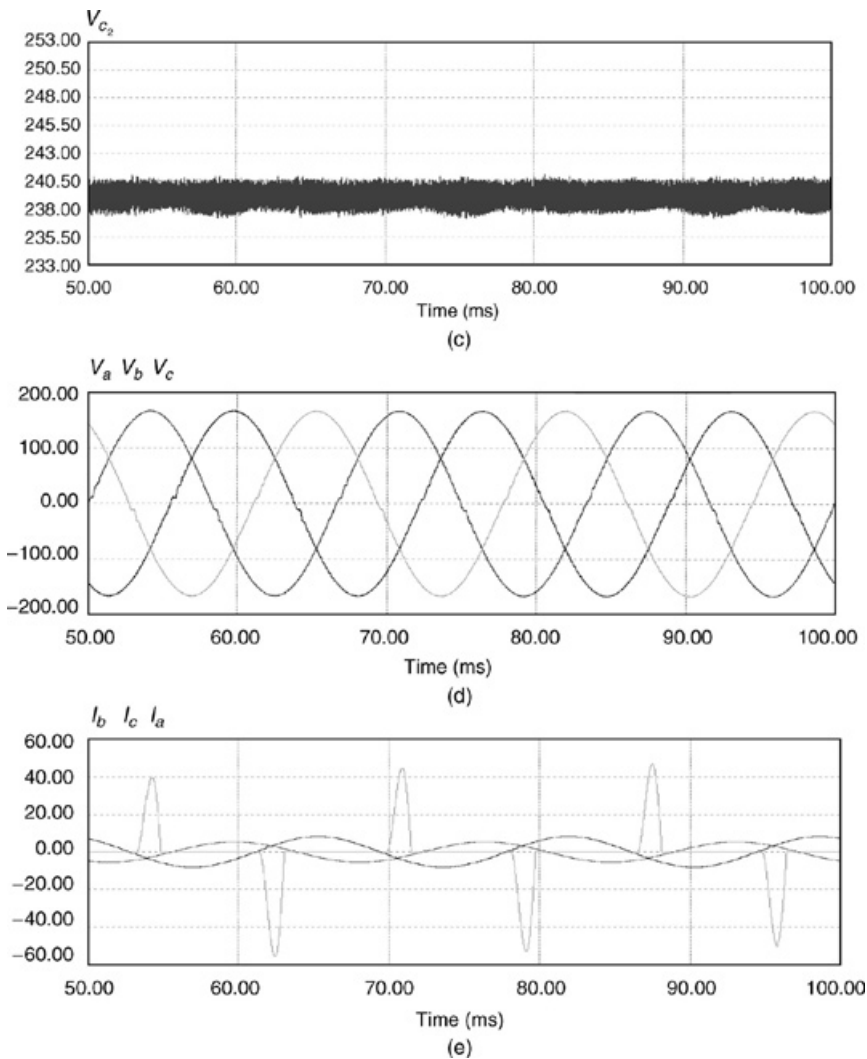


FIGURE 4.53 (continued)

- Excellent power-conditioning throughout the wide input voltage variation range in both amplitude and frequency.
- Small weight, size, and cost.

Apart from these, the use of the novel AC/DC rectifier yields the following advantages over the UPS systems based on the conventional half-bridge rectifier:

- Ability of full independent control over the two DC-link capacitor voltages in both the normal mode of operation and stored-energy mode of operation.

TABLE 4.2
Cost comparison between the proposed single-phase UPS system and its conventional counterpart

Component	Proposed UPS system (Fig. 4.32)				Conventional UPS system (Fig. 4.3)			
	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)
IGBT	S_1-S_4	4	35.00	140.00	S_1-S_6	6	35.00	210.00
	S_5	1	2.22	2.22				
Diode	D_1-D_4	4	2.90	11.60	—	—	—	0.00
	D_5	1	1.78	1.78	—	—	—	0.00
SCR	S_t	1	3.20	3.20	—	—	—	0.00
Static switch	S_{in}	1	6.40	6.40	S_{in}	1	6.40	6.40
	Bypass	1	6.40	6.40	Bypass	1	6.40	6.40
Inductors	L_s	1	26.00	26.00	L_s	1	26.00	26.00
	L_{dc}	1	8.21	8.21	L_{dc}	1	70.22	70.22
	L_o	1	5.25	5.25	L_o	1	5.25	5.25
Capacitors	C_1, C_2	2	18.30	36.60	C_1, C_2	2	18.30	36.60
Miscellaneous		1	50.00	50.00		1	50.00	50.00
Total cost				297.66				410.87
Total savings				113.21				-113.21

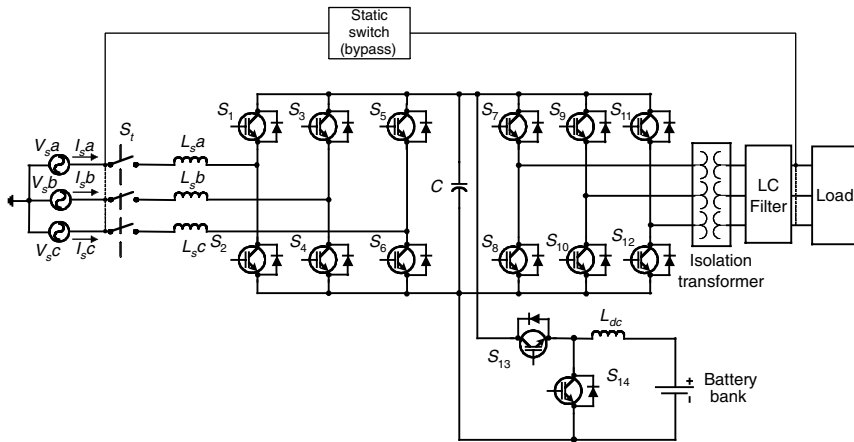
- Two times lower voltage stresses across the IGBTs in the front-end rectifier and boost converter.
- Higher efficiency and reliability.
- Lower number of active switches.

In sum, the proposed UPS systems in Section 4.3 with their compactness, low cost, and excellent performance are strong candidates for the optimal low-cost UPS systems for low-power applications, such as mainframe computers and servers.

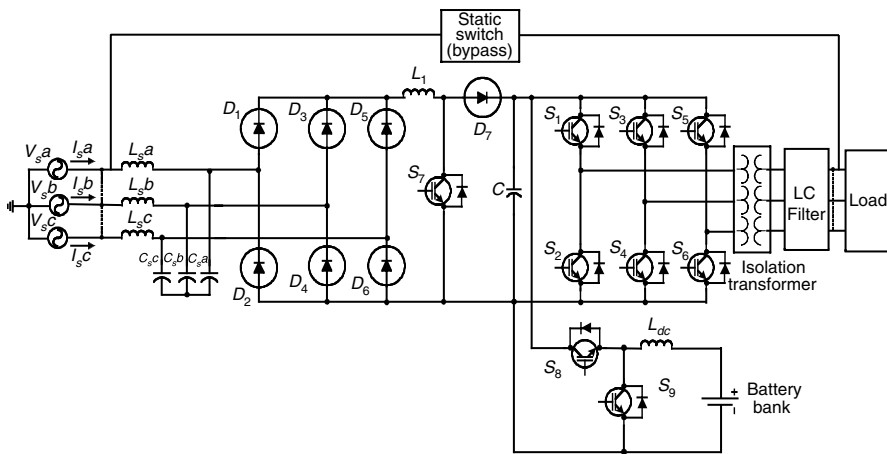
4.4 New Three-Phase On-Line UPS System with Reduced Number of Switches

While the on-line UPS systems are widely recognized as the superior topology in performance, power conditioning, and load protection, it should be mentioned that they use a large number of switches and as a consequence have a high cost. This is especially true for three-phase UPS systems. Typical three-phase on-line UPS systems are shown in Figure 4.54 and Figure 4.55.

The UPS system from Figure 4.54 has at its front-end a three-phase controlled AC/DC rectifier consisting of input inductors L_{sa} , L_{sb} , and L_{sc} , and six switches: S_1 to S_6 . It is controlled to charge the DC capacitor to a level sufficient for proper operation of the back-end inverter. At the same time, it can

**FIGURE 4.54**

Typical three-phase on-line UPS system with a controlled rectifier.

**FIGURE 4.55**

Typical three-phase on-line UPS system with an uncontrolled rectifier.

provide PFC. The PF correction control is of boost type, so the UPS system can work in the normal operation mode even when the input AC voltage is considerably lower than the nominal value.

The bidirectional DC/DC converter is the usual charger/discharger already described in [Chapter 1](#). The DC/AC inverter consists of six switches S_7 to S_{12} and an output LC filter. It is controlled in a high-frequency PWM pattern to give high-quality sinusoidal output voltage with a low THD. An isolation transformer is required for safety. The static switch is used to transfer the load directly to the AC line in case of UPS system failure or if maintenance is required. It can also be used to support fault clearance.

In the UPS system from Figure 4.55, a combination of an uncontrolled three-phase rectifier and a boost DC/DC converter replaces the controlled front-end rectifier. The uncontrolled rectifier consists of six diodes: D_1 to D_6 . Its purpose is to rectify the AC voltage. The boost converter consists of a DC inductor L_b , switch S_5 , and diode D_7 . Its purpose is to maintain the input current sinusoidal and in phase with the input AC voltages, providing in this way unity PF. The rest of the UPS system is the same as that from Figure 4.54.

A new three-phase on-line UPS system is proposed in this section. It has a reduced number of active switches compared to the conventional counterparts from Figure 4.54 and Figure 4.55, and in fact eliminates the need for a separate boost converter for the battery. Its configuration is shown in Figure 4.56.

4.4.1 System Description

The new UPS system, shown in Figure 4.56, constitutes a front-end uncontrolled AC/DC rectifier, followed by a PFC boost converter, a half-bridge type DC/AC inverter with an isolation transformer, a battery charger, a battery bank, a transfer switch S_i in the form of thyristor, and a bypass static switch.

The uncontrolled rectifier consists of six diodes: D_1 to D_6 . It rectifies the AC voltage, while the boost converter at the back-end of the rectifier is in charge of providing PFC. It consists of a DC inductor L_b , switch S_5 , and diode D_7 .

The DC/AC inverter consists of a split DC bus, and four switches S_1 , S_2 , S_3 , and S_4 , as well as an isolation transformer and an output LC filter. It operates in a high-frequency SPWM pattern in order to provide high-quality sinusoidal output voltage.

The battery charger is a DC/DC buck converter, which consists of switch S_6 , diode D_8 , and DC inductor L_{dc} . Its purpose is to step down the high DC bus voltage to low battery voltage, thus controlling the charge of the battery bank.

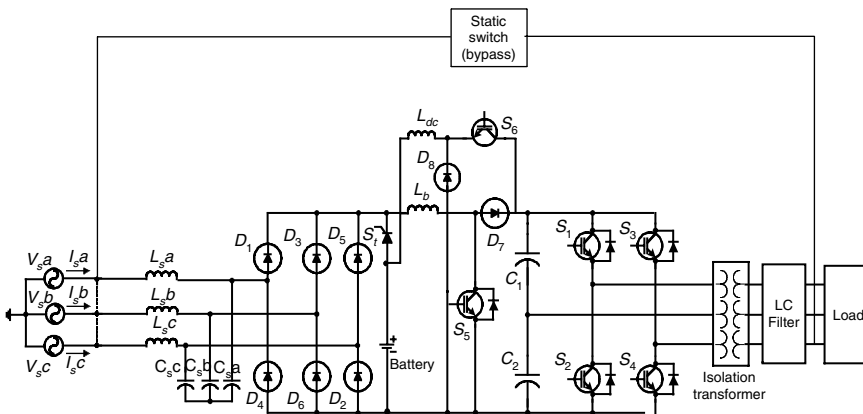


FIGURE 4.56

Proposed three-phase on-line UPS system with reduced number of switches.

The transfer switch S_t is used to transfer the input power source from the AC line to the battery. The bypass static switch is used in case of failure or if maintenance is required. In order to ensure unnoticeable transfer from normal to bypass mode and vice versa, the inverter output voltage must be in phase with the AC line voltage.

4.4.2 Basic Principles of Operation

The proposed UPS system has three operating modes: normal mode, stored-energy mode, and bypass mode. In the normal mode of operation, the input AC voltage is within the permissible tolerance range. The power is passed from the AC/DC rectifier to the DC/AC inverter and the load is continuously supplied with high-quality AC power. The DC/DC buck converter charges the battery and maintains it at 100% state of charge (SOC). The transfer switch S_t is off.

The three-phase uncontrolled rectifier followed by a PFC boost converter has been investigated by Prasad et al. [14]. The circuit operates in DCM and its essence is in transferring energy from the input capacitors C_{sa} , C_{sb} , and C_{sc} to the DC-link inductor L_b and vice versa.

The three-phase rectifier works in the following way. When switch S_5 is turned on, the input line voltage is applied across the boost inductor L_b and the corresponding currents in the phases start increasing/decreasing according to

$$V_m \sin(\omega t) = L_1 \frac{di}{dt} \quad (4.30)$$

When switch S_5 is turned off, the energy stored in the boost inductor L_b is transferred through diode D_7 to the DC-link charging capacitors C_1 and C_2 . Since the current shaping converter is of a boost type, the DC-link bus voltage is always larger than the maximum amplitude value of the input voltage and as a result the voltage across the boost inductor L_b is negative. The input phase currents start decreasing/increasing according to

$$V_m \sin(\omega t) = L_1 \frac{di}{dt} + V_{dc} \quad (4.31)$$

The input phase currents change with a rate proportional to the instantaneous value of their corresponding input phase voltages, and their peak values are also proportional to the average value of their corresponding phase voltages. Since these voltages are sinusoidal, then the peak currents will also be sinusoidal. Keeping in mind that the rectifier works in discontinuous conduction mode, the average values of the input currents will be sinusoidal. In summary, the input currents consist of high-frequency harmonics and low-frequency fundamental harmonics at 60 Hz. Removing the high-frequency harmonics is easily achievable with a small electromagnetic interference (EMI) filter. The current shaping switch S_5 operates at constant frequency. The duty cycle varies with the load to ensure a tightly regulated DC-link bus voltage.

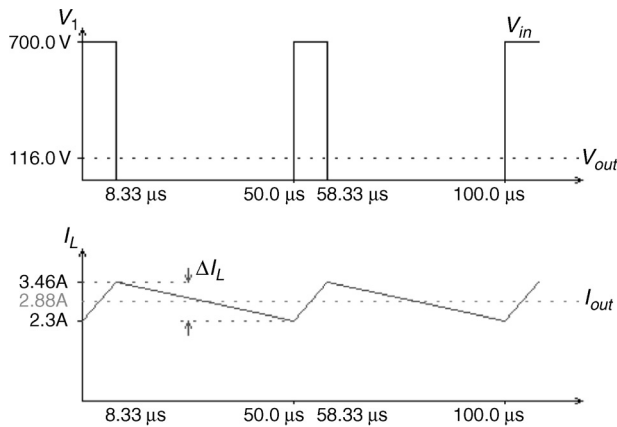


FIGURE 4.57
Operation of the battery charger.

The battery charger is a typical buck DC/DC converter. Figure 4.57 depicts the voltage across diode D_8 , the current through inductor L_{dc} , and the output voltage V_{out} across the battery terminals [12].

The DC/AC three-phase inverter consists of a split DC-link capacitor bus and two IGBT legs, with switches S_3 , S_4 and S_5 , S_6 . It is controlled in a high-frequency PWM pattern to yield a high-quality sinusoidal output voltage with low THD. A three-phase AC voltage system is obtained from the four-switch inverter by using sinusoidal PWM control strategy where the control signals for the two legs are 120° phase shifted from each other. Since the line voltage V_{ab} is 120° shifted from the line voltage V_{bc} , and they are equal in amplitude, inherently the line voltage V_{ca} is 120° shifted from V_{bc} , completing the symmetrical system of line voltages V_{ab} , V_{bc} , V_{ca} , which are 120° shifted to one another, as shown in Figure 4.58 [5].

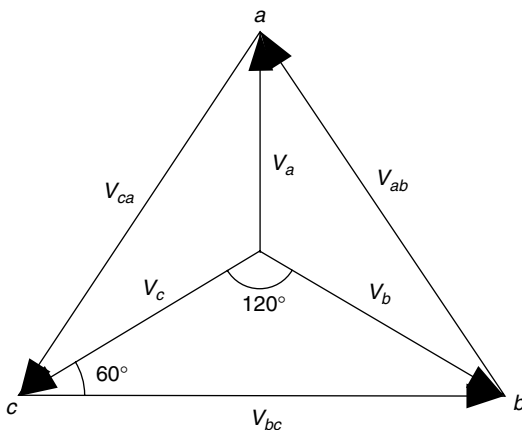


FIGURE 4.58
Symmetrical system of line voltages V_{ab} , V_{bc} , and V_{ca} .

The control strategy for the three-phase inverter uses two control loops for each inverter leg: one outer voltage loop and one inner current loop. The outer control loop uses the output line voltage as a feedback signal, which is compared with a reference signal. The two reference signals for the two legs are phase shifted 120° from each other. The error is compensated by a *PI* integrator to achieve stable output voltage under steady-state operation. This error is also used as a reference signal for the inner current regulator loop, which uses the output inductor current as a feedback signal. The minor current loop is much faster than the outer voltage loop, and improves the dynamic response of the inverter. As a result, the output voltage has a very high quality even with a highly non-linear load.

In the stored-energy mode of operation, when the input AC voltage is beyond the permissible tolerance range, switch S_i is turned on, transferring the input from the AC line to the battery bank. The boost converter used in the normal operation mode for current shaping is now used for boosting the low battery voltage to high DC-link bus voltage. When switch S_5 is turned on, the voltage across inductor L_b is positive and the current through it starts to increase. When switch S_5 is turned off, the current through inductor L_b follows the path $V_{bat}^+ - L_b - D_6 - C_1 - C_2 - V_{bat}^-$ and charges DC-link capacitors C_1 and C_2 . The low battery voltage is a function of the battery voltage and the duty ratio of switch S_5 is

$$V_{dc} = \frac{V_{bat}}{1-D} \quad (4.32)$$

Figure 4.59 shows the voltage across switch S_5 , the output voltage V_{out} across the DC-link bus, the current through inductor L_b , and the current through diode D_7 [12].

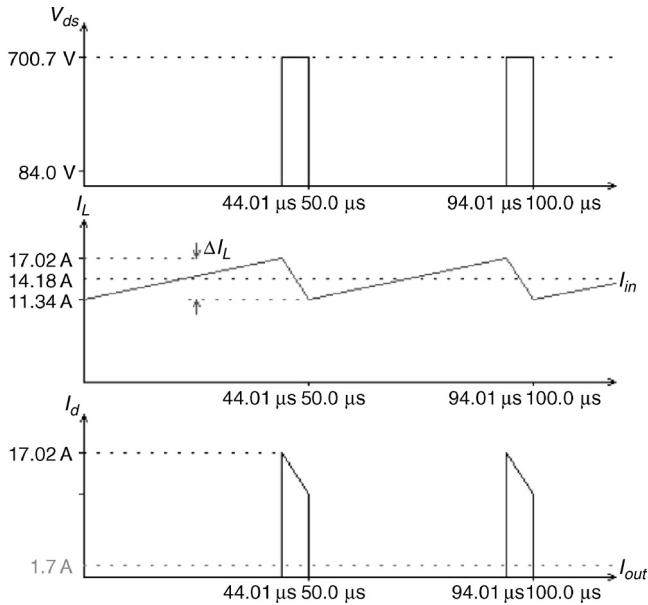
The operation of the DC/AC inverter in the stored-energy mode is the same as that in the normal operating mode.

4.4.3 Simulation Results

Various computer simulations have been carried out, using PSIM simulation software, to help design the control for the new UPS system.

The system parameters have been chosen as follows:

- Input voltage: Three-phase 120 VAC $\pm 25\%$
- Battery voltage: 96 V
- DC-link bus voltage: 700 V (2×350 V)
- Output voltage: 3×120 VAC $\pm 5\%$ or/and 3×208 VAC $\pm 5\%$
- Output frequency: 60 Hz $\pm 0.5\%$
- THD: $< 5\%$
- Output power: 1 kVA continuous
- Switching frequency: 20 kHz

**FIGURE 4.59**

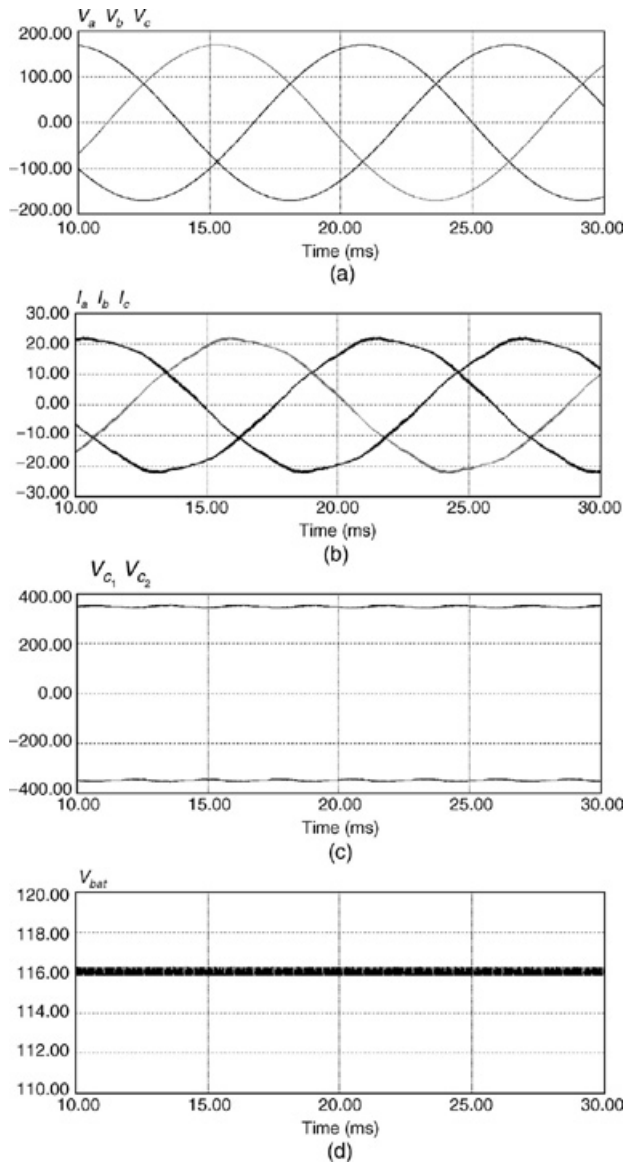
Operation of the DC/DC step-up converter.

After careful design considerations, described in Section 4.2.1.3, regarding the input current PF and THD, DC-link voltage ripples, and cut-off frequency of the output low-pass filter, the following values for the passive components have been chosen:

- $L_b = 1.82 \text{ mH}$
- $C_e = 0.03 \text{ } \mu\text{F}$
- $C_1 = 4700 \text{ } \mu\text{F}$
- $C_2 = 4700 \text{ } \mu\text{F}$
- $L_{dc} = 2.22 \text{ mH}$
- $L_o = 100 \text{ } \mu\text{H}$
- $C_o = 20 \text{ } \mu\text{F}$

The simulation results for normal mode of operation for the proposed UPS system are shown in Figure 4.60. The input phase currents I_a , I_b , and I_c are sine waves in phase with the corresponding input AC voltages V_a , V_b , and V_c , resulting in PF very close to unity. The DC-link bus voltage is regulated at 700 V or 350 V for each capacitor C_1 and C_2 . At the same time, the battery charger steps down the high DC-link bus voltage to the low battery charging voltage of 116 V. The back-end DC/AC inverter continuously supplies the load with a high-quality three-phase voltage.

The simulation results for the stored-energy mode of operation for the proposed UPS system are shown in Figure 4.61. The boost converter works

**FIGURE 4.60**

Simulation results for normal mode of operation. (a) Input phase voltages V_a , V_b , and V_c , (b) input phase currents I_a , I_b , and I_c , (c) DC-link voltages, (d) battery voltage V_{bat} , (e) battery current I_{bat} , (f) output phase voltages V_a , V_b , and V_c , and (g) load phase currents I_a , I_b , and I_c .

in DCM and it steps up the low battery voltage from 96 V to a high DC-link bus voltage of 700 V. The three-phase voltage system generated by the back-end inverter is of very high quality with very little THD.

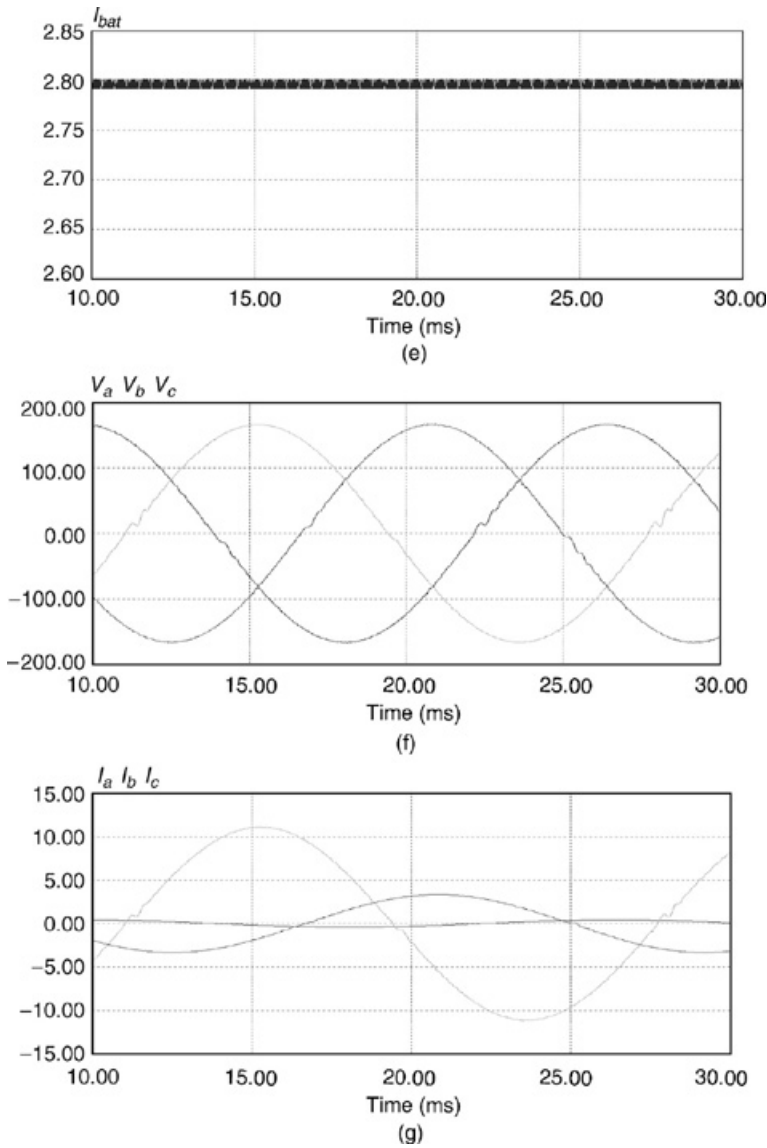
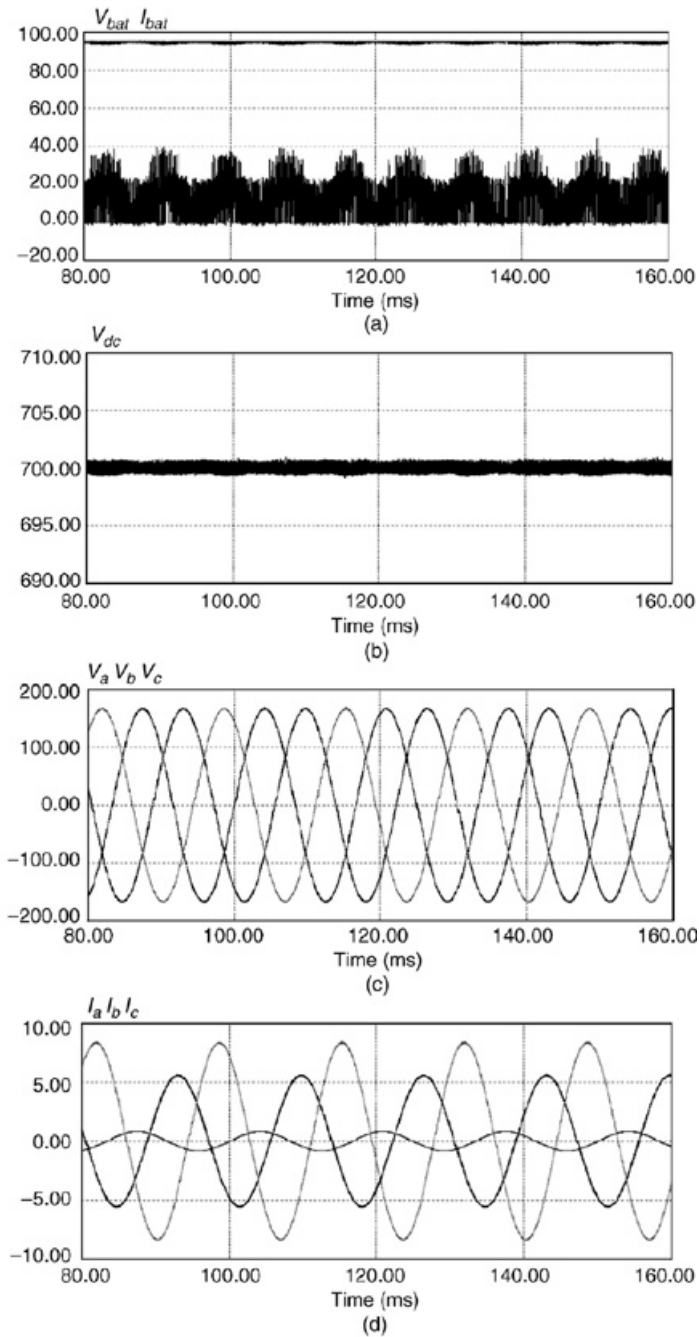
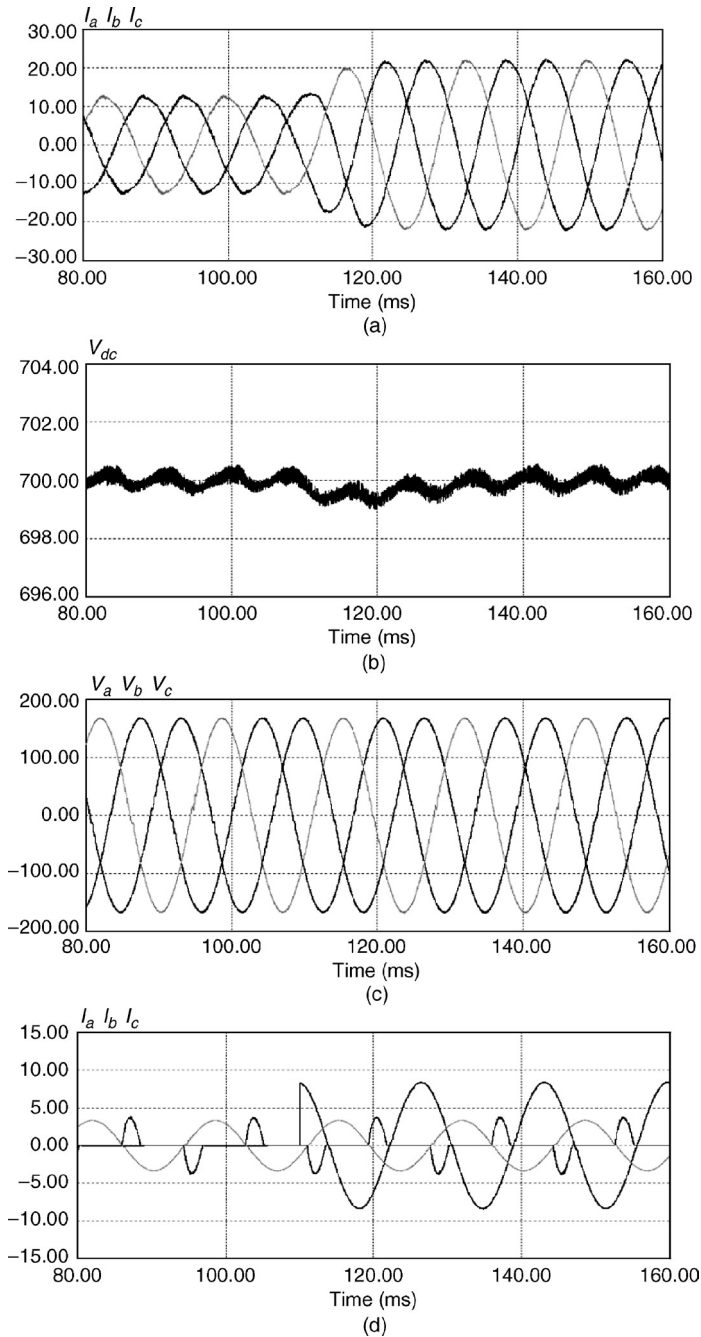


FIGURE 4.60 (Continued)

Finally, [Figure 4.62](#) shows the dynamic performance of the proposed UPS system in the normal mode of operation with step-changing load. Phase A feeds a standard nonlinear load — 150 W rectifier. Phase B feeds 300 W resistive load, and phase C initially works at no load and after 0.11 s 650 W resistive load is connected. It can be observed by the results that the dynamic performance of the proposed system is excellent. The input currents are maintained sinusoidal. The DC-link bus voltage only dips 1.5 V and recovers

**FIGURE 4.61**

Simulation results for stored-energy mode of operation. (a) Battery voltage V_{bat} and battery current I_{bat} , (b) DC-link bus voltage V_{dc} , (c) output phase voltages V_a , V_b , and V_c , and (d) load phase currents I_a , I_b , and I_c .

**FIGURE 4.62**

Simulation results for normal mode of operation with step-changing load. (a) Input phase currents I_a , I_b , and I_c . (b) DC-link bus voltage V_{dc} . (c) output phase voltages V_a , V_b , and V_c . (d) load phase currents I_a , I_b , and I_c .

within a cycle. Finally, the output voltages do not experience any distortion at the time of connection of the load.

4.4.4 Performance Analyses and Cost Evaluation

When evaluating the performance of the proposed UPS system, the first point to underline is the excellent quality of the output voltage supplied to the critical load. The THD of the three-phase voltage systems is below 2.5% even with highly nonlinear and nonsymmetrical loads. The second point that needs to be stressed is the exceptional dynamic performance and stability of the proposed UPS system with step-changing loads.

Another performance characteristic to highlight is the superb PF, which is kept close to unity even when the UPS system feeds highly nonlinear and nonsymmetrical loads. The proposed UPS system not only possesses excellent performance characteristics but is also less expensive when compared to the conventional counterparts due to the elimination of the step-up DC/DC converter and the use of a four-switch DC/AC inverter instead of the conventional six-switch inverter. As shown in Table 4.3, the overall cost savings for the proposed three-phase on-line UPS system is \$177.89 or 23% compared to the conventional counterpart from Figure 4.55. As already mentioned, in an extremely competitive market, such as the low and middle power class UPS systems, the cost issue is of increasingly high importance. Last but not least, it should be noted

TABLE 4.3
Cost comparison between the proposed three-phase UPS system and its conventional counterpart

Component	Proposed UPS system (Fig. 4.56)				Conventional UPS system (Fig. 4.55)			
	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)
IGBT	S_1-S_4	4	35	140	S_1-S_9	9	35	315
	S_5	1	7.63	7.63				
	S_6	1	18.9	18.9				
Diode	D_1-D_6	6	2.165	12.99	D_1-D_6	6	2.165	12.99
	D_7	1	4.03	4.03	D_7	1	4.03	4.03
	D_8	1	2.16	2.16	—	—	—	0
SCR	S_t	1	3.2	3.2	—	—	—	0
	Bypass	1	19.2	19.2	Bypass	1	19.2	19.2
Inductors	L_b	1	71.22	71.22	L_b	1	43.99	43.99
	L_{dc}	1	8.21	8.21	L_{dc}	1	70.22	70.22
	L_o	3	5.25	15.75	L_o	3	5.25	15.75
Capacitors	C_1, C_2	2	18.3	36.6	C_1, C_2	2	18.3	36.6
Transformer		1	185.96	185.96		1	185.96	185.96
Miscellaneous		1	70	70		1	70	70
Total cost				595.85				773.74
Total savings				177.89				-177.89

that the reduced number of components combined with the low battery voltage increases the reliability of the whole system.

4.4.5 Conclusions

The proposed three-phase on-line UPS system has many performance features characteristic only for the high-end quality truly state-of-the-art UPS systems, such as:

- High-quality sinusoidal output voltages even with highly nonlinear and nonsymmetrical loads.
- Unity input power factor.
- Excellent transient characteristics and stability.
- Small weight, size, and cost.

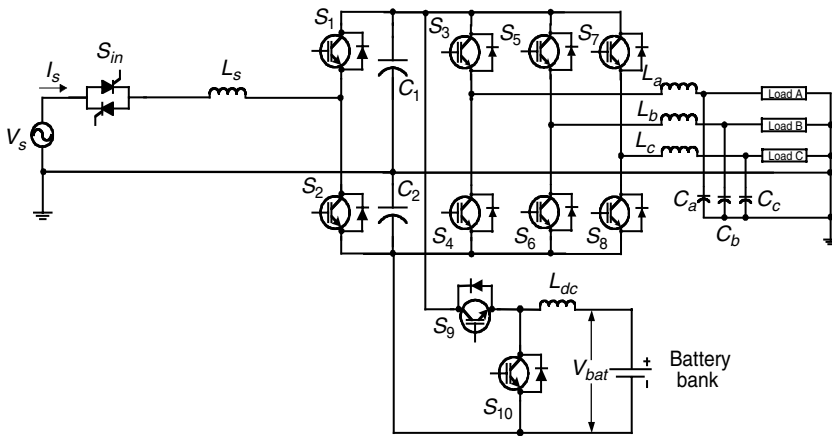
By making use of the fact that the uncontrolled rectifier at the front-end of the UPS system is followed by a boost DC/DC converter for PFC purposes, the conventional boost converter, used for boosting the low battery voltage, has been eliminated, which results in a substantial cost, weight, and size savings without any compromise in the performance.

Additional cost savings have been realized by using a four-switch DC/AC inverter topology instead of the conventional six-switch inverter topology. In sum, the proposed three-phase on-line UPS system with its compactness, low cost, and excellent performance is a strong candidate for the optimal low-cost UPS system for low to middle power applications, such as PCs and servers.

4.5 New Single-Phase to Three-Phase Hybrid Line-Interactive/On-Line UPS System

When a three-phase power supply is required in the presence of only single-phase power, the typical approach is to use the on-line topology shown in [Figure 4.63](#). Although on-line UPS systems are widely recognized as superior in performance, they have some drawbacks. The first drawback is its low efficiency due to the fact that it requires double conversion of the electrical power: from AC to DC and after that from DC to AC. The second drawback is its high cost due to the large number of switches employed.

Line-interactive UPS systems have a simpler design and as a consequence a higher reliability and lower cost compared to on-line UPS systems. Another advantage of line-interactive UPS systems is their higher efficiency compared to the on-line topology, which comes inherently from the single conversion nature of line-interactive topology.

**FIGURE 4.63**

Typical single-phase to three-phase on-line UPS system.

In this section, a new single-phase to three-phase hybrid line-interactive/on-line UPS system with reduced number of switches is proposed.

Reduced-parts single-phase to three-phase converters for motor drives application, with PFC capabilities, have been proposed by Enjety et al. and Chen et al. [15, 16]; but the concept has not yet been applied to UPS systems. The new single-phase to three-phase UPS system proposed in this chapter applies the concept of reduced-parts converters to line-interactive UPS topology. Its configuration is shown in [Figure 4.64](#).

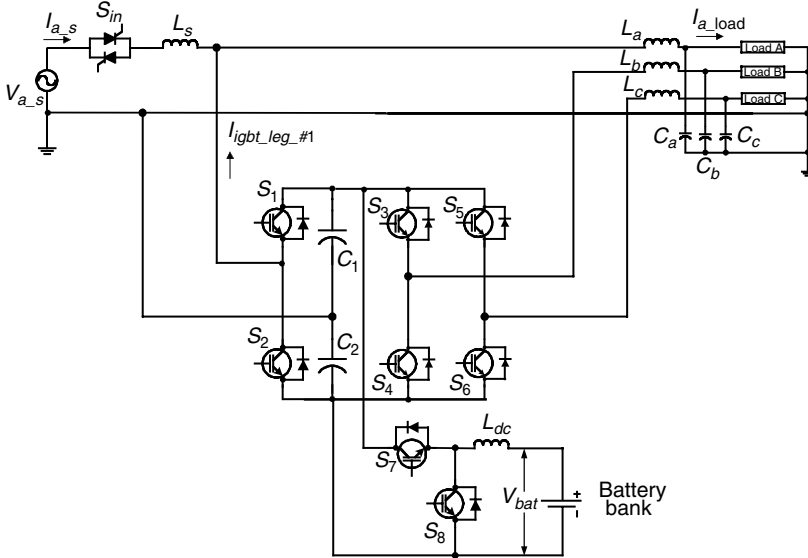
4.5.1 System Description

The new UPS system, shown in [Figure 4.64](#), is based on half-bridge converter topology. It consists of an input switch S_{in} , an input inductor L_s , and three IGBT legs connected to a split DC-link bus and a bidirectional DC/DC converter, which functions as a battery charger/discharger.

One of the IGBT legs is connected in parallel to the AC line and can act during the normal operating mode as a shunt active filter. It is also in charge of conditioning the AC power to the load connected in phase A when there are disturbances in the input voltage. The input inductor L_s serves as a buffer between the input AC voltage and the load voltage.

The other two IGBT legs are operated in a high-frequency SPWM pattern in order to provide high-quality sinusoidal output voltages. The sinusoidal-modulating references for generating the PWM gate signals for the two legs are phase shifted at 120° between each other. In this way, a symmetrical three-phase voltage system is produced.

The bidirectional battery charger/discharger is used to charge the battery during the normal mode of operation, and to boost the low battery voltage to high DC-link bus voltage during the stored-energy mode of operation.

**FIGURE 4.64**

Proposed single-phase to three-phase hybrid UPS system with reduced number of switches.

The input switch is turned off during the stored-energy mode to prevent back feed of power to the AC line.

It should be mentioned that in the proposed design, there is no bypass switch. It was assumed that the proposed low-cost single-phase to three-phase UPS system would be most suitable for applications where a low-cost reliable three-phase power supply was needed in the presence of single-phase power supply only. Hence, it was implicit that there was no option of a redundant three-phase power supply by a bypass switch. If 99.999% availability is required, then the option of the so-called “ $N+1$ redundancy” can be investigated.

4.5.2 Basic Principles of Operation

The proposed new UPS system has two operating modes: normal operating mode and stored-energy operating mode. In the normal mode of operation, the input AC voltage is within the permissible tolerance range. The input switch is on and the power is passed directly from the AC line to the load in phase A. At the same time, the first IGBT leg with switches S_1 and S_2 works as a half-bridge rectifier and supplies the DC-link bus with power. The input inductor voltage drop is designed to be small under normal rated conditions; hence, the power factor is very close to unity under these conditions. It should be mentioned that during this operating mode, the UPS system cannot work as an active filter in the presence of nonlinear or RL load. In order to provide PFC, the UPS system needs to go to the stored-energy mode

of operation and draw energy from the battery since the first leg cannot work as a rectifier and as an active filter at the same time.

The other two IGBT legs work in inverter mode the same way as the back-end inverter described in Section 4.2.3 and feed the loads connected in phases B and C. The battery charger steps down the high DC-link voltage from 480 V to a tightly regulated 116 V in order to charge the batteries and maintain them at 100% SOC.

There are two submodes for the stored-energy mode of operation. During the first stored-energy submode, the first IGBT leg, which is connected to phase A, acts as an active filter in order to compensate for any undervoltage or overvoltage conditions, assuming they are within $\pm 10\%$ of the nominal voltage or to improve the input PF. We use the equivalent circuit for the fundamental frequency of phase A, as shown in Figure 4.65, to explain the power-conditioning function of the first IGBT leg.

The battery voltage and the amplitude modulation index m_a of the SPWM control determine the amplitude of V_1 generated by the first IGBT leg. This means that V_1 can be adjusted independent of the AC line voltage V_s . The shift angle δ between V_s and V_1 determines the real power flow.

We assume that the AC line voltage V_s is 100% of its nominal value and the output voltage V_1 is 100% of its nominal value as well. The shift angle δ between the two voltage vectors is determined by the real power demanded by the load.

$$P = \frac{V_s \times V_1 \times \sin \delta}{j\omega L} \quad (4.33)$$

As mentioned, the input inductor voltage drop is designed to be small under normal rated conditions and resistive load. It was chosen to be $\delta = 8^\circ$ for our design. Hence, the power factor is very close to unity under these conditions. Since $\cos \varphi = \cos (\delta/2)$, then for $\delta \cong 8^\circ$ the PF is 0.998. The phasor diagram for this case is shown in Figure 4.66.

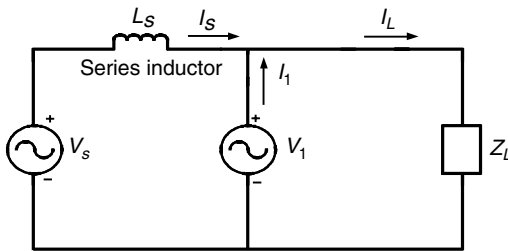


FIGURE 4.65
Equivalent circuit for the fundamental frequency.

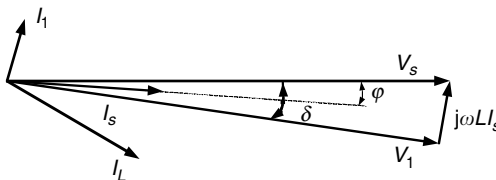


FIGURE 4.66
Phasor diagram for the equivalent circuit from Figure 4.66.

When working as an active filter, the first IGBT leg supplies only the reactive power necessary to compensate the reactive voltage drop across the series inductor and the reactive power consumed by the load. In fact, current drawn from the AC line can always be kept sinusoidal and in phase with the AC input voltage V_{a_s} , providing unity PF.

A diagram of the implemented control strategy for the IGBT leg working as an active filter is shown in Figure 4.67.

The principle of the output voltage regulation in the stored-energy mode can be easily understood with the help of the phasor diagrams in Figure 4.68 and Figure 4.69. The inverter supplies more reactive power for undervoltage conditions or less reactive power for overvoltage conditions. Keeping the angle between the inverter current I_1 and V_1 equal to 90° guarantees that the first inverter leg will supply only reactive power and no real power will be drawn from the battery for voltage compensation in phase A. During no severe voltage disturbances when the voltage is within $\pm 10\%$ of its nominal value, the power drawn from the battery will be only the power needed for the loads in phases B and C. In this way, the life of the battery is extended and the overall efficiency of the UPS system is increased.

When the AC line is not available or is beyond the preset tolerance of $\pm 10\%$, the three-leg converter works as a conventional three-phase DC/AC inverter and supplies the load with energy from the battery set. The

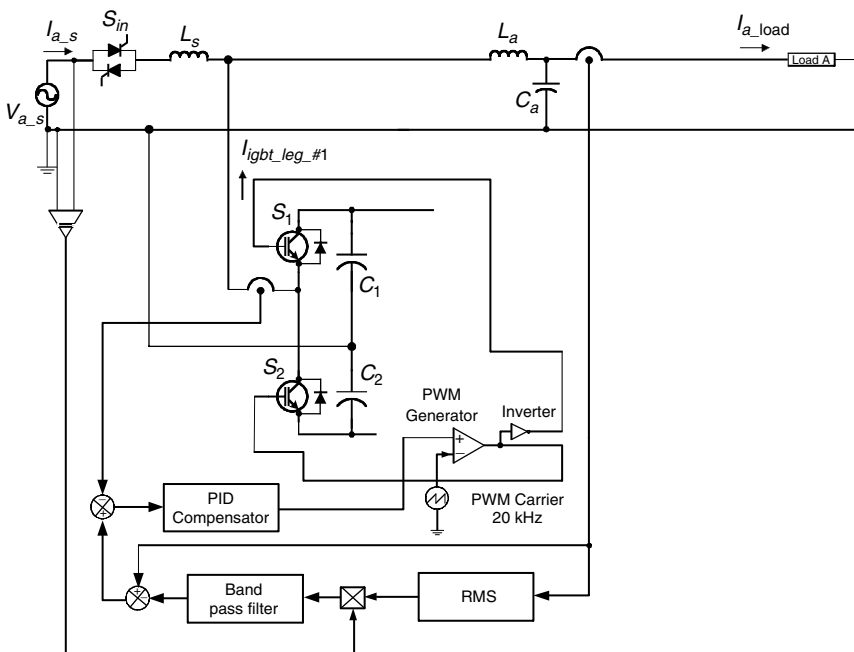
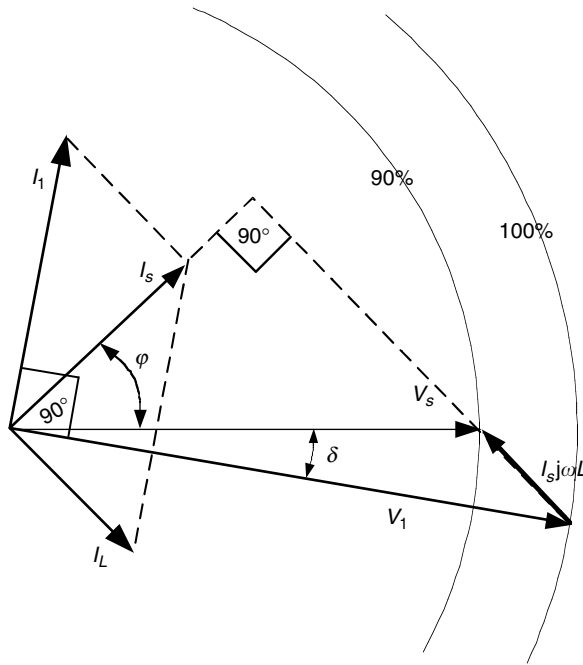


FIGURE 4.67

Control strategy for the first IGBT leg working as an active filter.

**FIGURE 4.68**

Phasor diagram for undervoltage conditions.

operation principles of the three-phase DC/AC inverter have been explained in Sections 4.2 and 4.3.

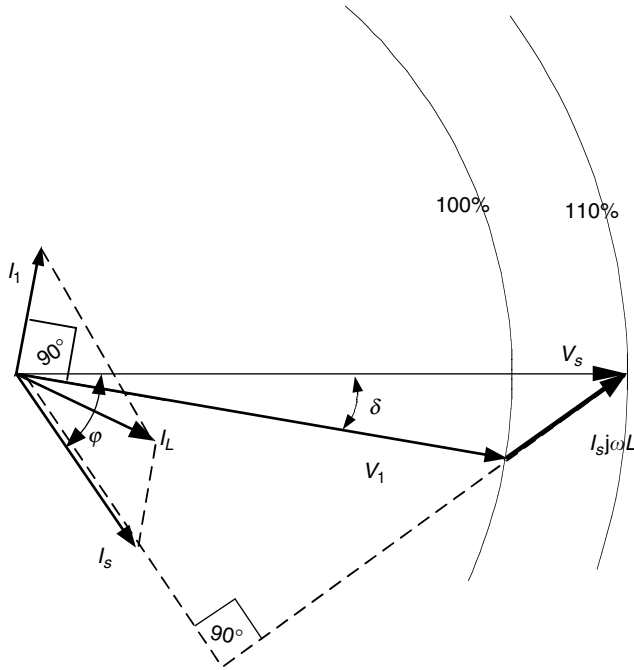
During the stored-energy mode of operation, the bidirectional converter works as a boost converter. It steps up the low battery voltage to high DC-link voltage for proper operation of the DC/AC inverter.

4.5.3 Simulation Results

Extensive computer simulations have been carried out, using PSIM simulation software, to help design the control for the new UPS system.

The system parameters have been chosen as shown below:

- Input voltage: Single-phase 120 VAC $\pm 10\%$
- Battery voltage: 96 V
- DC-link bus voltage: 480 V (2×240 V)
- Output voltage: 3×120 VAC $\pm 5\%$ or/and 3×208 VAC $\pm 5\%$
- Output frequency: 60 Hz $\pm 0.5\%$
- THD: $< 5\%$
- Output power: 1 kVA continuous
- Switching frequency: 20 kHz

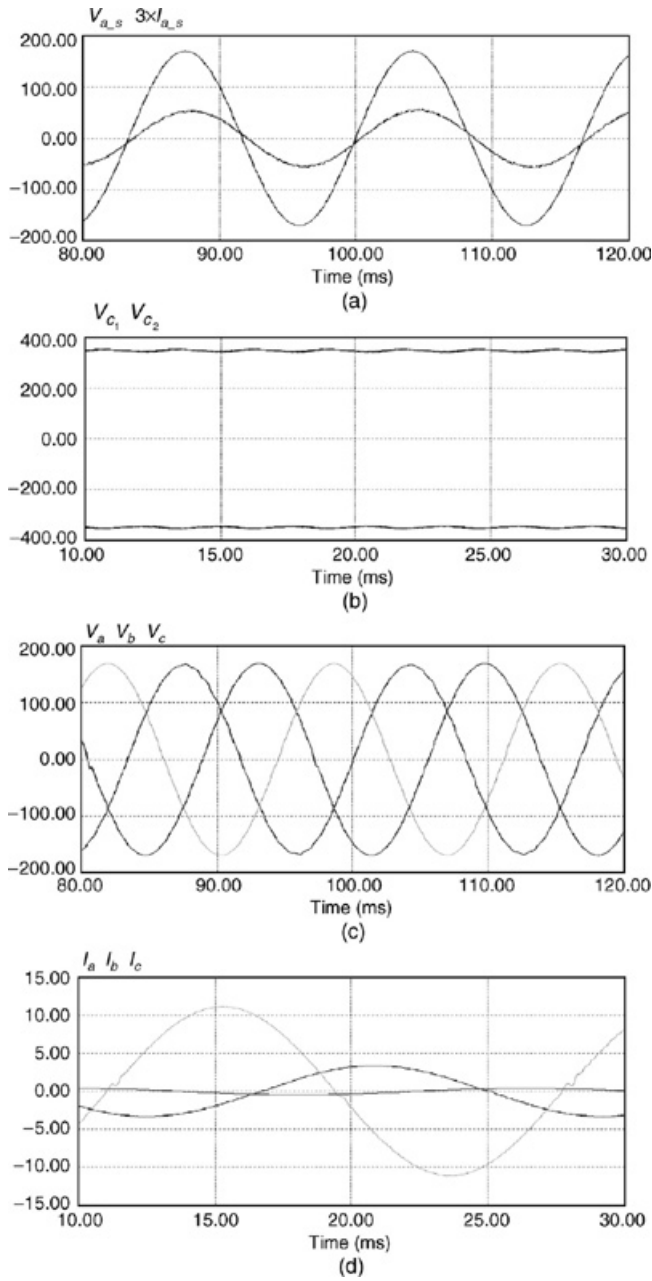
**FIGURE 4.69**

Phasor diagram for overvoltage conditions.

Three assumptions were made when calculating the value for the input inductance L_s . First, it is assumed that the proposed UPS system should provide voltage regulation within $\pm 10\%$ of input voltage variation. Second, the load has a power factor of no less than 0.8. The third assumption is that the reactive power, which the UPS system can produce, does not exceed the active power rated. After careful design considerations regarding the DC-link voltage ripples, and the cut-off frequency of the output low-pass-filter, the following values for the passive components L_s , C_1 , C_2 , L_{dc} , L_o , and C_o have been chosen.

- $L_s = 5 \text{ mH}$
- $C_1 = 4700 \text{ }\mu\text{F}$
- $C_2 = 4700 \text{ }\mu\text{F}$
- $L_{dc} = 2.22 \text{ mH}$
- $L_o = 100 \text{ }\mu\text{H}$
- $C_o = 20 \text{ }\mu\text{F}$

The simulation results for the normal mode of operation for the proposed UPS system with a resistive load of 1000 W are shown in [Figure 4.70](#). As can be seen, the three-phase voltage system has a very high quality with little

**FIGURE 4.70**

Simulation results for normal mode of operation. (a) Input phase voltage $V_{a,s}$ and current $I_{a,s}$ for phase A, (b) DC-link bus voltages V_{c1} and V_{c2} , (c) phase output voltages $V_{a'}$, $V_{b'}$, and $V_{c'}$, and (d) load phase currents I_a , I_b , and I_c .

THD. At the same time, PF is close to unity, although the first IGBT leg works as a rectifier in this operating mode and does not provide PFC. In fact, it is in charge of supplying the DC-link bus with the DC power necessary for generating the other two-phase voltages of a symmetrical three-phase system.

The simulation results for the first stored-energy submode of operation for the proposed UPS system are shown in [Figure 4.71](#). The first IGBT leg, which is connected to phase A, acts as an active filter and compensates for the non-linearity of the load to improve the input PF. A standard 300 W single-phase rectifier is connected to phase A. As observed from the simulation results, the proposed UPS system is capable of providing unity PF during this operating mode.

Simulation results for the bidirectional converter, which works as a boost converter in CCM and steps up the low battery voltage from 48 V to high DC-link bus voltage of 480 V are shown in [Figure 4.72](#).

[Figure 4.73](#) shows the simulation results for the same stored-energy submode of operation when the first IGBT leg provides PFC in the presence of 300 W inductive load. The first leg provides only the reactive power required by the load. As a result, the input PF is unity. The real power to the load in phase A is still provided by the AC line.

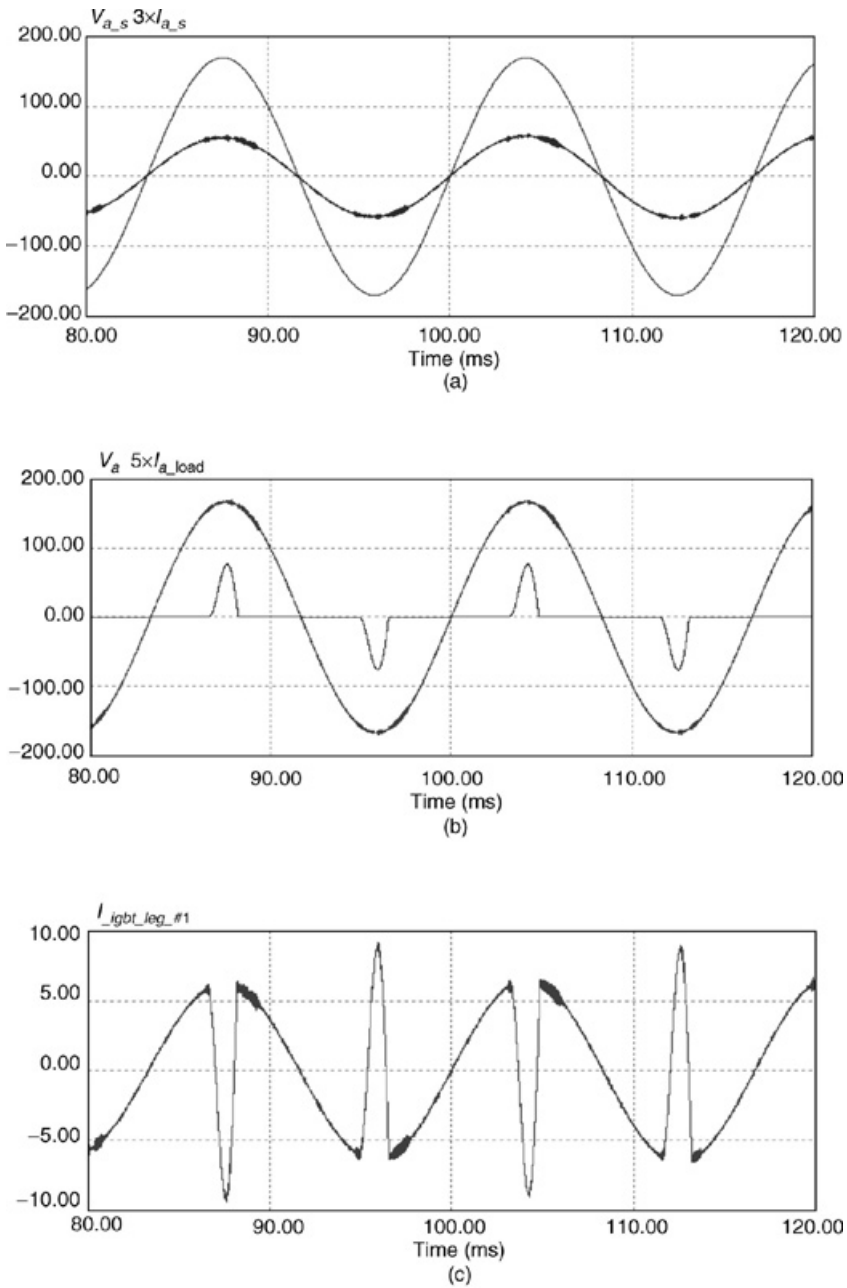
Finally, [Figure 4.74](#) shows the dynamic performance of the proposed UPS system with step-changing load in the stored-energy submode of operation when the first IGBT leg works as an active filter. Phase A initially feeds a 50 W resistive load and after 0.10 s, a 150 W rectifier is connected. Phase B feeds 300 W resistive load and phase C feeds 150 W resistive load. As can be observed by the results, the dynamic performance of the proposed system is excellent. The input current is kept sinusoidal in phase with the input AC voltage and the output voltages do not experience any distortion at the time of connection of the load.

4.5.4 Performance Analyses and Cost Evaluation

The proposed single-phase to three-phase hybrid line-interactive/on-line UPS system has excellent quality of the output voltage supplied to the critical load. The THD of the three-phase voltage systems is below 5% even with highly nonlinear loads. The simulation results for its dynamic performance and stability tested with step-changing loads reveal the advantages of the proposed multiple control loop strategies.

The proposed UPS system can work as an active filter in order to improve the input PF. It can also provide voltage compensation in undervoltage and overvoltage conditions within $\pm 10\%$ of the nominal voltage value.

The new UPS system not only possesses excellent performance characteristics but is also less expensive when compared to the conventional on-line single-phase to three-phase UPS system. As shown in [Table 4.4](#), the overall

**FIGURE 4.71**

Simulation results for stored-energy submode of operation when the first IGBT leg works as an active filter with 350 W rectifier load. (a) Input phase voltage $V_{a,s}$ and current $I_{a,s}$ for phase A, (b) output phase voltage V_a and load current $I_{a,load}$ for phase A, (c) current injected by the first IGBT leg for phase A, (d) modulation signal for gate pulses for the first IGBT leg connected in phase A, and (e) phase output voltages V_a , V_b , and V_c .

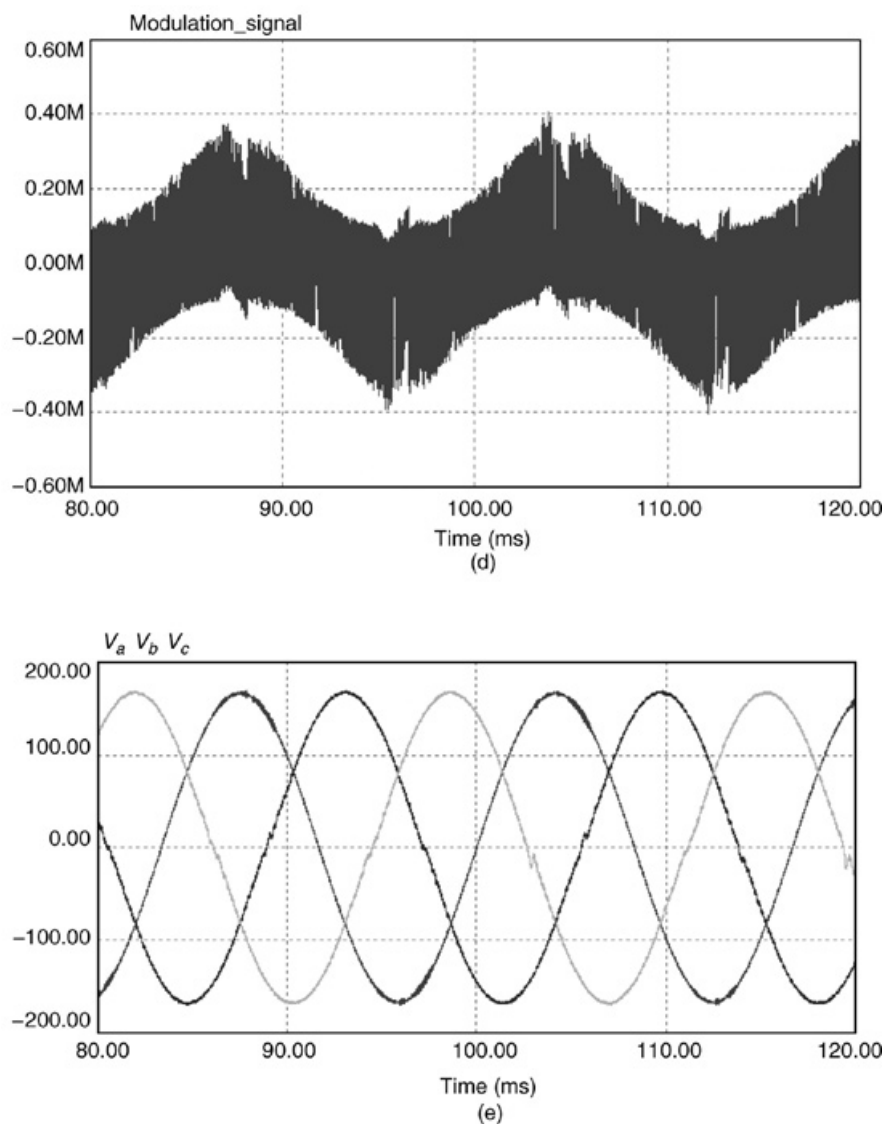
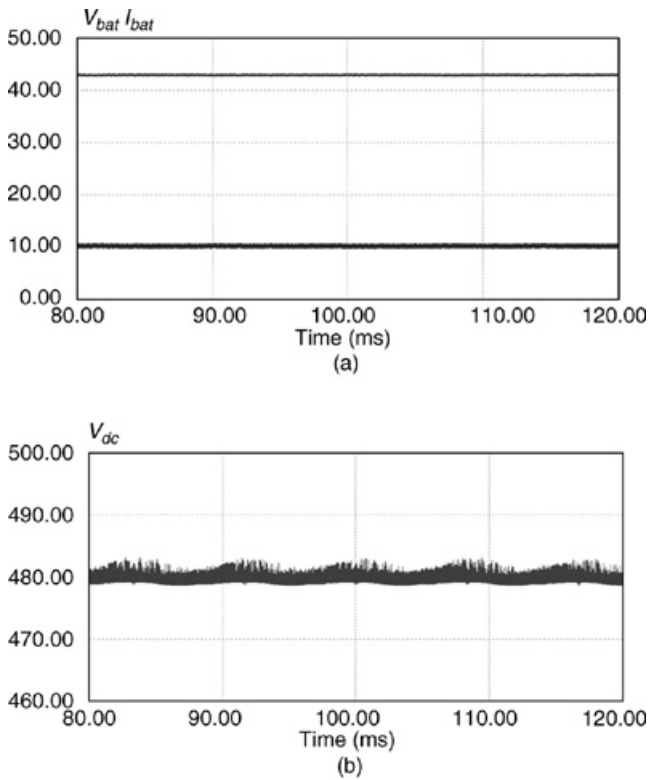


FIGURE 4.71 (Continued)

cost savings for the proposed three-phase on-line UPS system is \$44.50 or 8% compared to the conventional counterpart from Figure 4.63. As mentioned, in an extremely competitive market, such as the low and middle power class UPS systems, the cost issue is of increasingly high importance. Last but not least, it should be noticed that the reduced number of components combined with the low battery voltage increases the reliability of the whole system.

**FIGURE 4.72**

Simulation results for the bidirectional DC/DC converter in stored-energy mode of operation. (a) Battery voltage V_{bat} and battery current I_{bat} , and (b) DC-link bus voltage V_{dc} .

4.5.5 Conclusions

The proposed single-phase to three-phase hybrid line-interactive/on-line UPS system has many desirable performance characteristics, such as:

- High-quality sinusoidal output voltages, even with highly nonlinear and nonsymmetrical loads.
- Unity input power factor when PFC feature is enabled.
- Excellent transient characteristics and stability.
- Small weight, size, and cost.
- Higher efficiency compared to the conventional on-line counterpart.

In sum, the proposed single-phase to three-phase hybrid line-interactive/on-line UPS system is a very attractive low-cost high-efficiency solution for providing three-phase high-quality high-reliability uninterruptible power in the presence of single-phase power only.

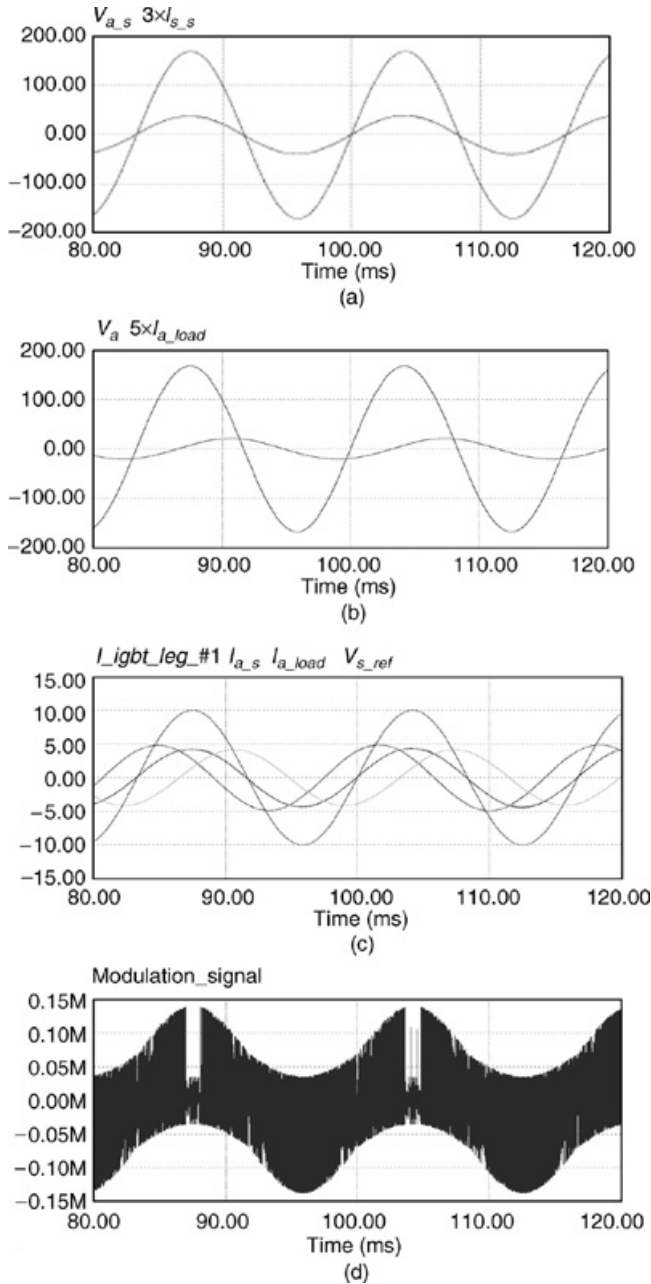
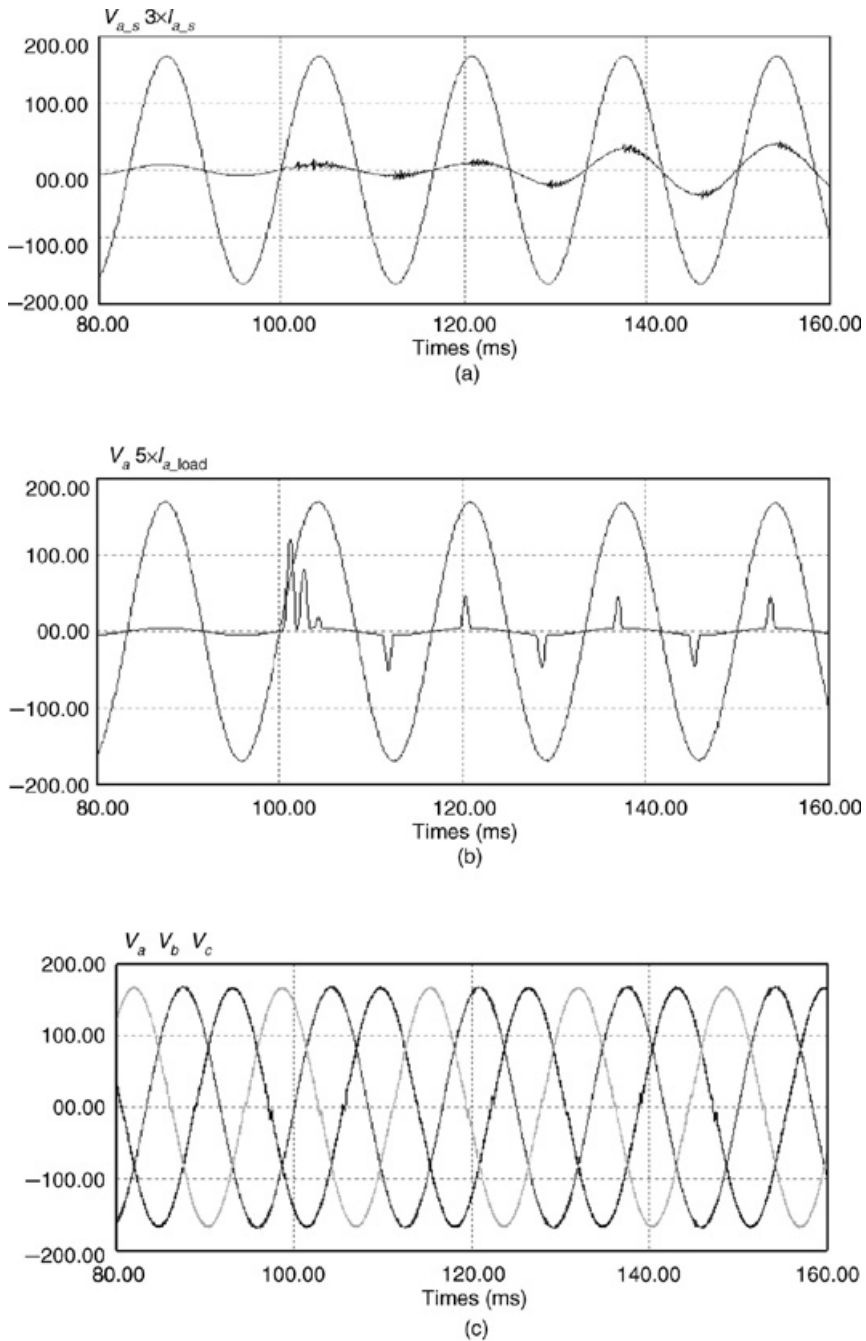


FIGURE 4.73

Simulation results for stored-energy submode of operation when the first IGBT leg works as an active filter with 300 W RL load. (a) Input phase voltage $V_{a,s}$ and current $I_{a,s}$ for phase A, (b) output phase voltage V_a and load current $I_{a,load}$ for phase A, (c) reference voltage $V_{s,ref}$, input current $I_{a,s}$, load current $I_{a,load}$, and compensating injected current for the first IGBT leg, and (d) modulation signal for gate pulses for the first IGBT leg connected in phase A.

**FIGURE 4.74**

Simulation results for stored-energy submode when the first IGBT leg works as an active filter and feeds step-changing load. (a) Input phase voltage $V_{a,s}$ and current $I_{a,s}$ for phase A, (b) output phase voltage V_a and load current $I_{a,load}$ for phase A, and (c) phase output voltages V_a , V_b , and V_c .

TABLE 4.4
Cost comparison between the proposed three-phase UPS system and its conventional counterpart

Component	Proposed UPS system (Fig. 4.64)				Conventional UPS system (Fig. 4.63)			
	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)	Desig.	Q'ty	Unit cost (\$)	Extended cost (\$)
IGBT	S_1-S_8	8	35.00	280.00	S_1-S_{10}	10	35.00	350.00
Static switch	S_{in}	1	6.40	6.40	S_{in}	1	6.40	6.40
Inductors	L_s	1	51.50	51.50	L_s	1	26.00	26.00
	L_{dc}	1	70.22	70.22	L_{dc}	1	70.22	70.22
	L_o	3	5.25	15.75	L_o	3	5.25	15.75
Capacitors	C_1, C_2	2	18.30	36.60	C_1, C_2	2	18.30	36.60
Miscellaneous		1	50.00	50.00		1	50.00	50.00
Total cost				510.47				554.97
Total savings				44.50				-44.50

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5

Reduced-Parts Active Filters

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Reducing the number of power electronic components in an active filter topology decreases the cost of the system. Additionally, the reduced number of switches results in fewer control functions and equipment and increasing system reliability. It should be noted, however, that the voltage utilization is worse and the performance of the system deteriorates.

5.1 Reduced-Parts Single-Phase and Three-Phase Active Filters

Figure 5.1 shows a half-bridge single-phase shunt active filter. It has two power electronic switches less than the full-bridge configuration; but the voltage of DC-link is twice the one in a full-bridge system. A reduced-part three-phase shunt active filter is shown in Figure 5.2. It also has two switches less than full-bridge configuration. i_{fa} and i_{fc} are controlled in the system and due to symmetry of the system i_{fb} is being controlled. Similarly, a reduced-parts single-phase series active filter is shown in Figure 5.3.

5.2 Reduced-Parts Single-Phase Unified Power Quality Conditioners

As discussed in the previous chapters, active filters are the best tools for harmonic mitigation as well as reactive power compensation, load balancing, voltage regulation, and voltage flicker compensation. Unified power quality conditioners (UPQC), also known as universal active filters, are ideal devices for improving power quality. The topology of three-phase UPQC systems was discussed in the last chapter. Different topologies of single-phase UPQC topologies are discussed in this section.

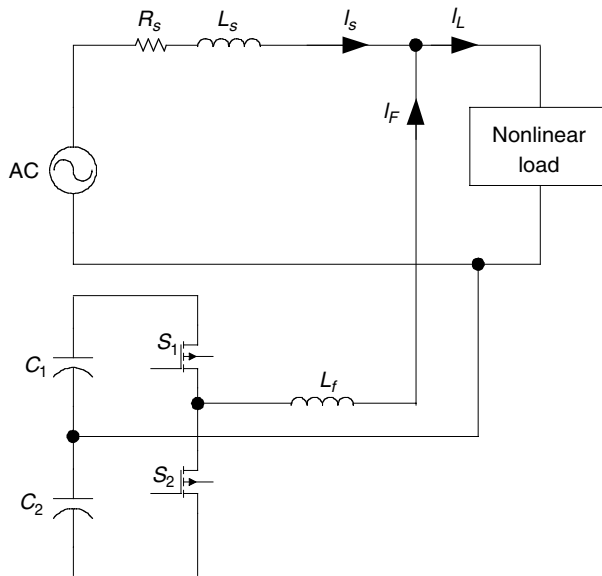


FIGURE 5.1
Reduced-parts single-phase shunt active filter.

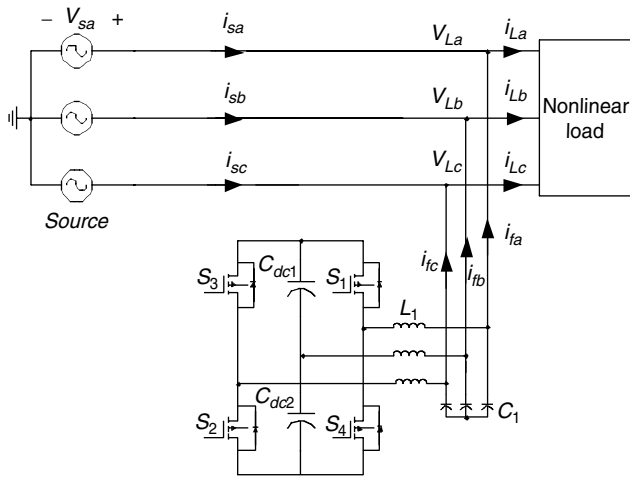


FIGURE 5.2
Reduced-parts three-phase shunt active filter.

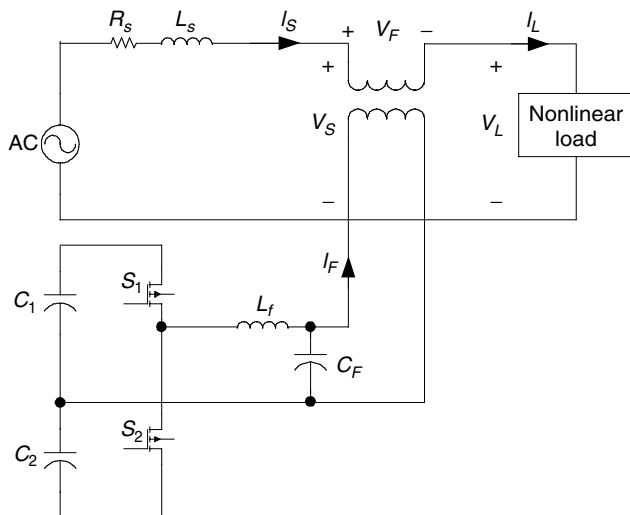
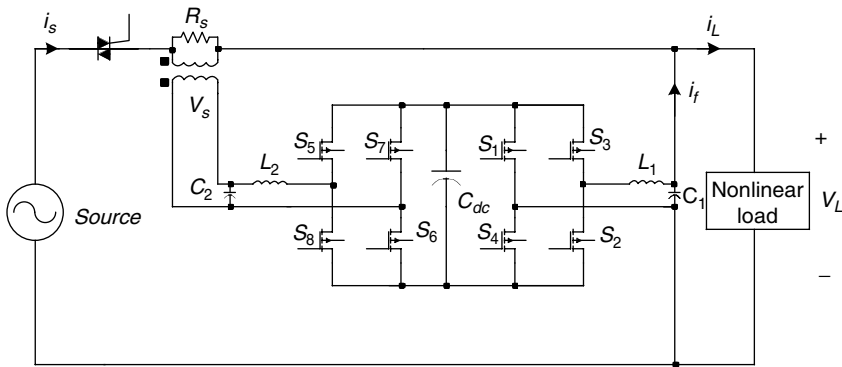


FIGURE 5.3
Reduced-parts single-phase series active filter.

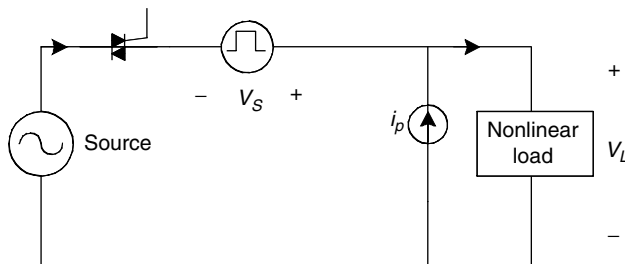
5.2.1 Single-Phase UPQC with Two Full-Bridge Converters

A conventional UPQC topology consists of two full-bridge bidirectional converters connected to a common DC-link bus, as shown in Figure 5.4. The series bidirectional converter consists of four switches. It is connected via a transformer in series with the AC line. The parallel bidirectional converter also consists of four switches. Two passive filters formed by L_1, C_1, L_2 , and C_2

**FIGURE 5.4**

A full-bridge single-phase UPQC.

remove switching frequency harmonics from the output current of the parallel converter and the output voltage of the series converter, respectively. L_1 also acts as a link between the filter and the system. The parallel converter delivers its current to the system through this inductor. Its inductance directly influences the bandwidth of the parallel converter. Load is a sensitive nonlinear electronic device. The series converter compensates the voltage difference of the input and reference voltage and regulates the voltage of the load terminal. This converter has the ability to cancel voltage disturbances such as harmonics, voltage sags and swells, and spikes. It gives or absorbs active power in the case of voltage sags and swells, respectively. For compensating the voltage harmonic of the source side, it only delivers reactive power. The parallel inverter mitigates the load's current harmonics, compensates the reactive current, and draws a small component of the fundamental current to recharge the DC-link capacitor. Figure 5.5 and Figure 5.6 show the equivalent circuit of the system and phasor diagram of the currents and voltages. Different operating modes of the system are discussed in this chapter.

**FIGURE 5.5**

Equivalent circuit of a single-phase UPQC system.

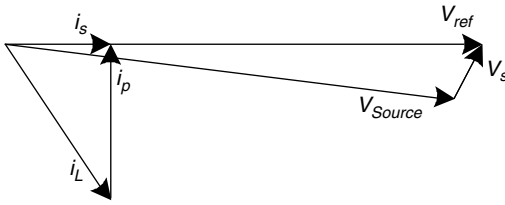


FIGURE 5.6

Phasor diagram of the currents and voltages of the system.

5.2.1.1 Voltage Control

In a UPQC system, two functions can be defined for the series converter. When the load is sensitive and critical, a series converter is used to regulate the line voltage for the load. It cancels out any line voltage distortions such as voltage harmonics, sag, swell, and voltage unbalance. It is capable of eliminating any voltage harmonics with a frequency within the bandwidth of the control scheme. After harmonic compensation of the parallel converter, the line current is considered free of harmonics. In this case, for compensating voltage harmonics, there is no need for active power. However, small components of harmonics remain in the line current. Passing through the terminal of the series converter, these current harmonics produce active power. The active power produced charges the DC-link capacitor. For voltage sag (swell) compensation, active power must be delivered to (received from) the system. This active power is supplied (received) by the DC capacitor and creates a voltage ripple on the DC bus voltage.

The second function of the series converter of a UPQC, which is mostly considered in very high power applications, is defined to protect the power system against the voltage distortions originating from the load. Some nonlinear loads, which usually have a capacitor bank after the bridge rectifier, appear to be voltage harmonic generators. The voltage harmonics at the point of common coupling (PCC) affect the other sensitive loads connected to this point. The series converter is capable of suppressing the voltage harmonics of the load.

A phase lock loop (PLL) is used to produce the reference voltage. The input of the PLL is the line voltage. The output of the PLL is a 60 Hz reference voltage, which is exactly in phase with the line voltage. Figure 5.7 shows the block diagram of the voltage control of the series converter. G_1 is the transfer function of the PI controller. The time constant of this controller is in the order of the switching frequency, and its minimum gain should be determined from the following equation:

$$|dv_{PWM}/dt| < |dv_{tri}/dt| = 4V_{tri}f_{sw} \quad (5.1)$$

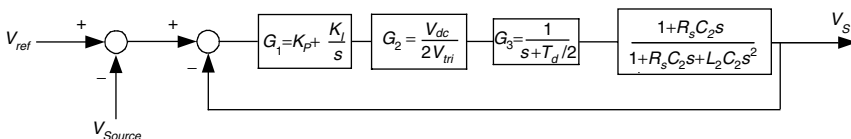


FIGURE 5.7

Block diagram of the voltage control of the series converter.

where G_2 is the gain of the PWM converter and G_3 is the time delay caused by the pulse width modulation (PWM) inverter. T_d is the switching period. G_4 models the delay of the output voltage of the series converter from output voltage of the PWM inverter. The resonance frequency of C_2 and L_2 is much higher than the switching frequency. R_s is a large resistor to remove any possibility of resonance. The transfer function from the reference voltage to the output current is as given in Equation 5.2. Figure 5.8 shows the frequency response of the series converter. The bandwidth of the transfer function is about 9000 rad/sec, which is more than the frequency range of the voltage disturbances in the power system.

$$\frac{V_s}{V_{ref}} = \frac{\frac{V_{dc}}{2V_{tri}}[K_p R_s C_2 s^2 + (K_I R_s C_2 + K_p) + K_I]}{L_2 C_2 s^3 + \left(\frac{V_{dc}}{2V_{tri}} K_p R_s C_2 + R_s C_2\right) s^2 + \left[\frac{V_{dc}}{2V_{tri}} (K_p + K_I R_s C_2) + 1\right] s + \frac{V_{dc}}{2V_{tri}} K_I} \quad (5.2)$$

The maximum single-phase voltage sag duration can be achieved from the following equation.

$$t_{\max} = \frac{1/2C_{dc}(V_{dc}^2 - V_{dcmin}^2)}{V_s I_L \cos \theta} \quad (5.3)$$

where V_{dcmin} is the minimum permissible voltage on the DC capacitor and θ is the power factor of the load.

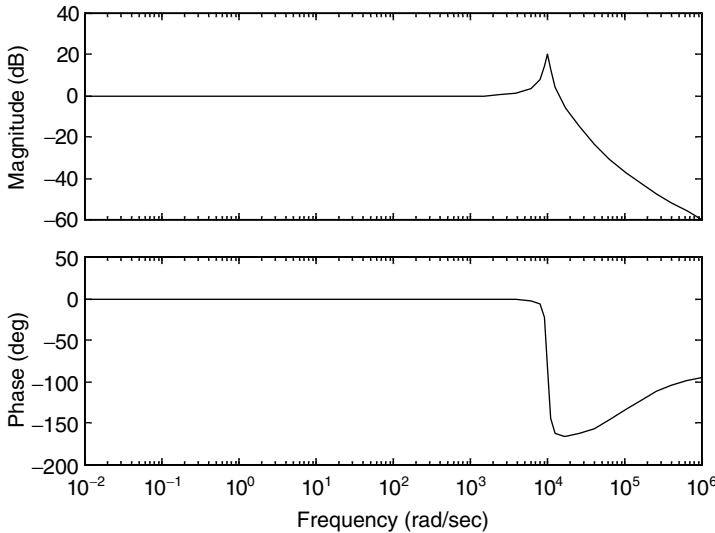


FIGURE 5.8

Frequency response of the series converter.

5.2.1.2 Current Control

Figure 5.9 shows the block diagram of the current control of the parallel converter. i_f^* is composed of three components: current harmonics of the load, reactive current of the load, and active current to compensate the loss and adjust the voltage of the DC capacitor. The parallel converter injects the same magnitude of harmonics in the reverse direction to make the current of the source side harmonic free. The transfer function of the current of the parallel converter to the reference current is as follows:

$$\frac{i_f}{i_f^*} = \frac{K_p s + K_I}{\frac{2V_{tri}}{V_{dc}} L_2 S^2 + K_p s + K_I} \quad (5.4)$$

Figure 5.10 shows the frequency response of the parallel converter. The bandwidth is mostly affected by L_2 . Bandwidth increases when the inductor decreases. On the other hand, when the inductor decreases, current harmonics

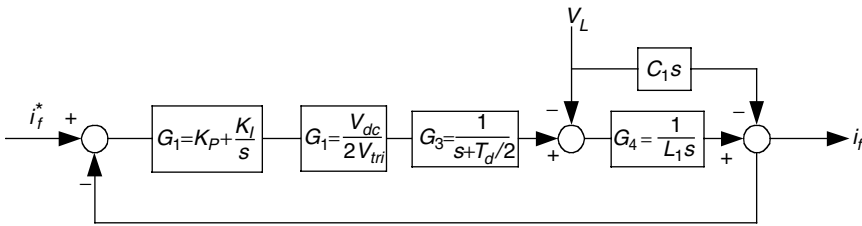


FIGURE 5.9

Block diagram of the current control of the parallel converter.

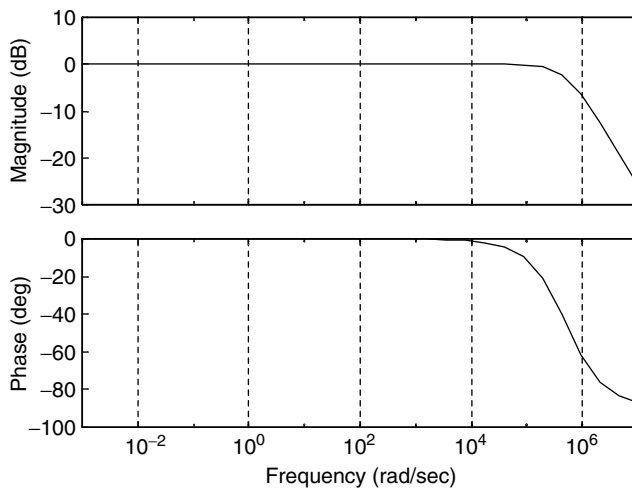


FIGURE 5.10

Frequency response of the parallel converter.

with switching frequency appear in the line current. Therefore, an appropriate value must be chosen for this inductor. A *PI* controller is used to control the voltage of the DC-link. Fundamental current is needed to recharge the capacitor. The voltage of the DC bus changes because of the losses in the system. The real power from the power system to the active filter is

$$P_{in} = V_a I_1 \quad (5.5)$$

where I_1 is the current with fundamental frequency. Power loss in the capacitor is equal to:

$$P_c = \frac{dW_c}{dt} = \frac{1}{2} c \frac{dV_{dc}^2}{dt} = c V_{dc} \frac{dV_{dc}}{dt} \quad (5.6)$$

From Equations 5.5 and 5.6, we obtain

$$\frac{V_{dc}}{I_1} = \frac{V_a}{c V_{dc} S} \quad (5.7)$$

The voltage control block diagram of the DC capacitor is shown in Figure 5.11. The low-pass filter cancels out any spike or AC disturbance from the DC voltage of the DC bus. The time constant of this *PI* controller must be much larger than the time constant of the *PI* controller for the current. Multiplying the output of the controller by the line voltage ensures that the fundamental component of the line current is used for charging the battery. Simulation results of the current regulation are shown in Figure 5.12.

5.2.2 Single-Phase UPQC with Two Half-Bridge Converters

A UPQC topology, based on two half-bridge bidirectional converters connected to a common DC-link, is an attractive solution in cost-sensitive low-power UPQC systems. The series bidirectional converter consists of two switches connected to a split DC bus, composed of two capacitors C_{dc1} and C_{dc2} . The parallel bidirectional converter also consists of two switches.

The reduced number of switches and control functions result in a price lower than that of a full-bridge-based topology. It should be noted, however, that the voltage utilization is worse and the harmonic content of the output is higher. A series-parallel UPQC topology based on two half-bridge bidirectional converters connected to a common DC-link bus is shown in Figure 5.13. The control strategy of this system is the same as the four-leg

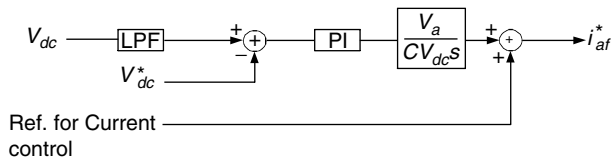


FIGURE 5.11

Block diagram of the voltage control.

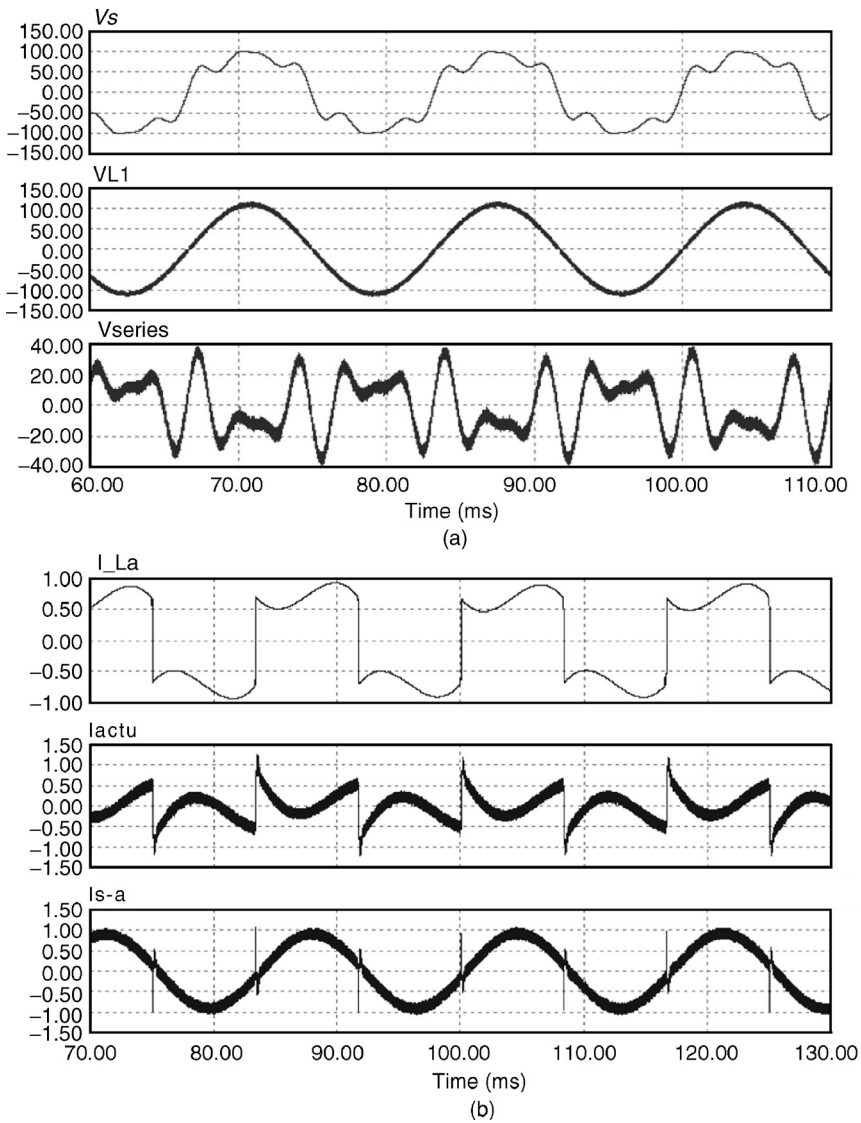


FIGURE 5.12 Simulation results of the full-bridge UPQC: (a) line and load voltage, and (b) load and line current.

converter. Figure 5.14 shows the simulation results of the system in the presence of voltage and current harmonics.

5.2.3 Single-Phase UPQC with Three Legs

The three-leg AC/DC/AC converter topology has drawn the attention of researchers in recent years and has been applied to many systems to achieve

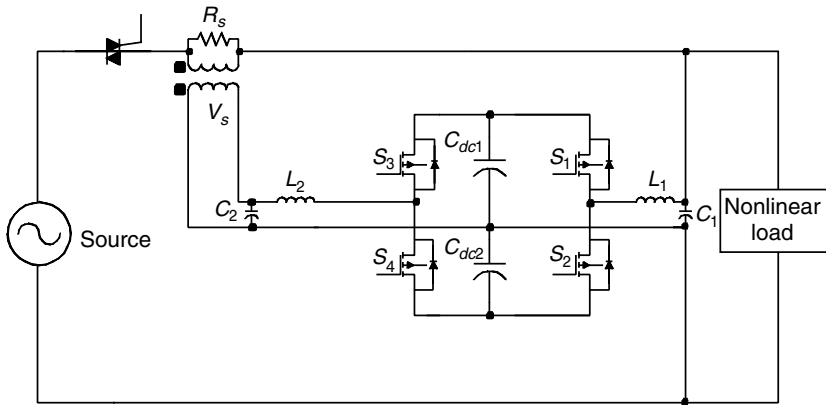
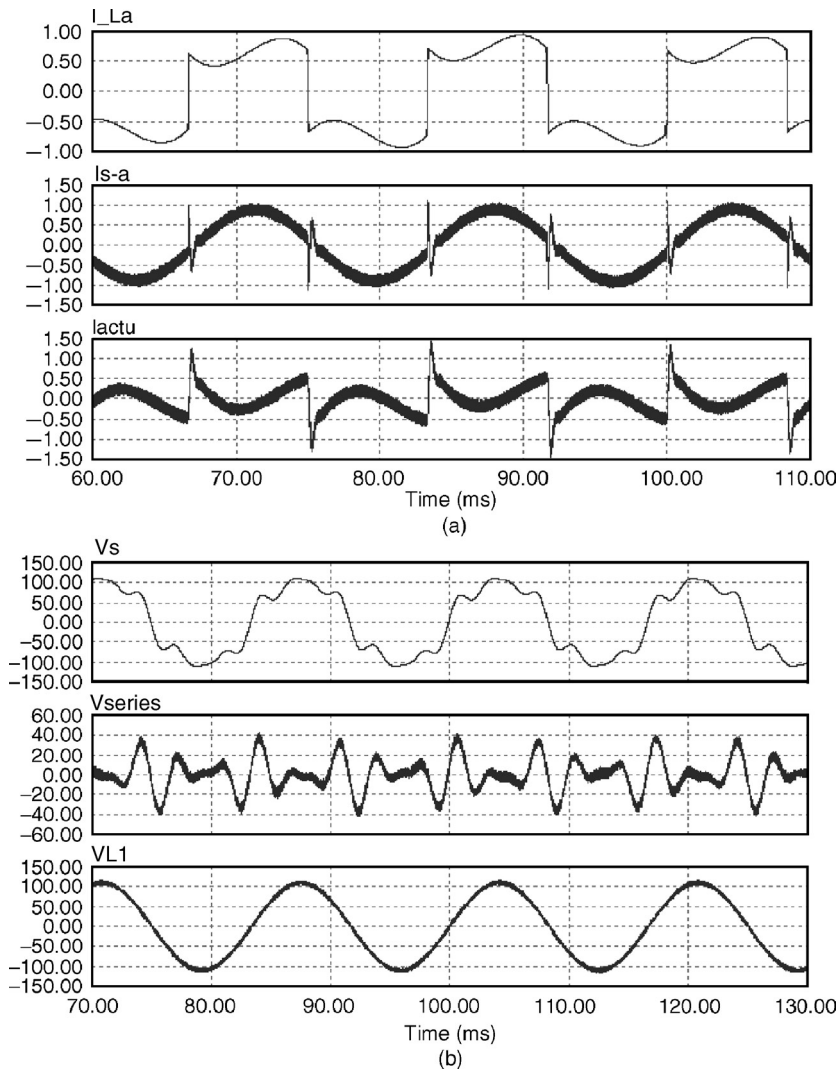


FIGURE 5.13
A half bridge single-phase UPQC.

a low cost and high performance at the same time. In an active filter system, for the controllability of the system, the voltage of the DC bus must be $\frac{3}{2}$ times the peak voltage of the line. In a half-bridge converter of the last section, the voltage of both capacitors C_{dc1} and C_{dc2} must be $\frac{3}{2}$ times the peak voltage of the line voltage. Therefore, the voltage of the capacitor must be three times the line peak voltage. In the three-leg converter, the voltage of the DC bus is the same as the voltage in the four-leg converter. However, the three-leg AC/DC/AC converter has not been applied to the UPQC topology yet. A UPQC topology based on the three-leg UPQC system is shown in Figure 5.15. The series bidirectional converter consists of the first leg, switches S_1 and S_4 . The parallel bidirectional converter consists of the third leg, switches S_5 and S_6 . The second leg, switches S_2 and S_3 , is common for both series and parallel converters.

In this topology, one of the converters is considered as the main converter depending on the priority of the system. Usually, the regulated voltage for the load is the first priority; the series converter is considered as the main converter. The series converter regulates the line voltage and makes a sinusoidal voltage for the load. The operation of this converter is the same as the series converter in Sections 5.2.2 and 5.2.3. In this mode, the parallel converter has limitations. The operation of the parallel converter depends on the operation of the series converter. S_5 can be turned on when S_2 is on and S_6 can be turned on when S_3 is on. The performance of the system varies with the control method. In the hysteresis control method, when the line voltage is in normal condition, the series converter is off and the parallel converter can work independently. In the PWM control technique, the series converter is always on. Therefore, the parallel converter is not independent. Table 5.1 shows the switching pattern of the system.

In fact, in the system, we always deal with periodic signals. Even most of the voltage disturbances within the range of 20% of the line voltage such as

**FIGURE 5.14**

Simulation results of the half-bridge UPQC: (a) line and load voltage, and (b) load and line current.

sag, swell, and harmonics are periodic. Therefore, the system works properly. Figure 5.16 shows the simulation results of the system.

If the line current harmonic compensation is of the first priority for the system, the parallel converter is considered as the main converter and it works the same as in Section 5.1. The operation of the series converter depends on the switching function of the parallel converter. Simulation results of the series converter are shown in Figure 5.17.

Typical experimental results of three systems are shown in Figure 5.18, Figure 5.19 and Figure 5.20. The circuit parameters of the three systems are

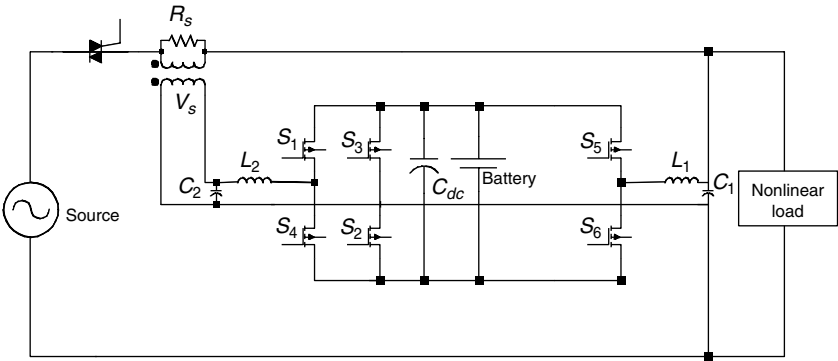


FIGURE 5.15
A three-leg UPQC topology.

TABLE 5.1
Switching pattern of the three-leg UPS

S_1	S_3	S_5	S_6
ON	OFF	ON/OFF	OFF
OFF	ON	OFF	ON/OFF

TABLE 5.2
Parameters of the Circuit

P_{Load}	C_{dc}	L	C_1	L_2	C_2
650 W	460 μF	1 mH	4.7 μF	0.1 mH	2.7 μF

shown in Table 5.2. Experimental results for the line voltage swell compensation and voltage harmonic cancellation for the full-bridge system are shown in Figure 5.18. Voltage and current harmonic mitigations of a half-bridge system are shown in Figure 5.19. Voltage and current harmonic compensations of the three-leg system are shown in Figure 5.20.

5.3 Reduced-Parts Single-Phase Series–Parallel Configurations

The same topology of UPQC works as an uninterruptible power supply (UPS) system with a battery pack in the DC bus. UPS systems protect critical loads against power disturbances from the main AC power supply. They provide a reliable uninterrupted high-quality power. Applications of UPS systems include life-supporting systems, data storage and computer systems, medical facilities, emergency equipment, telecommunications, and industrial processing systems.

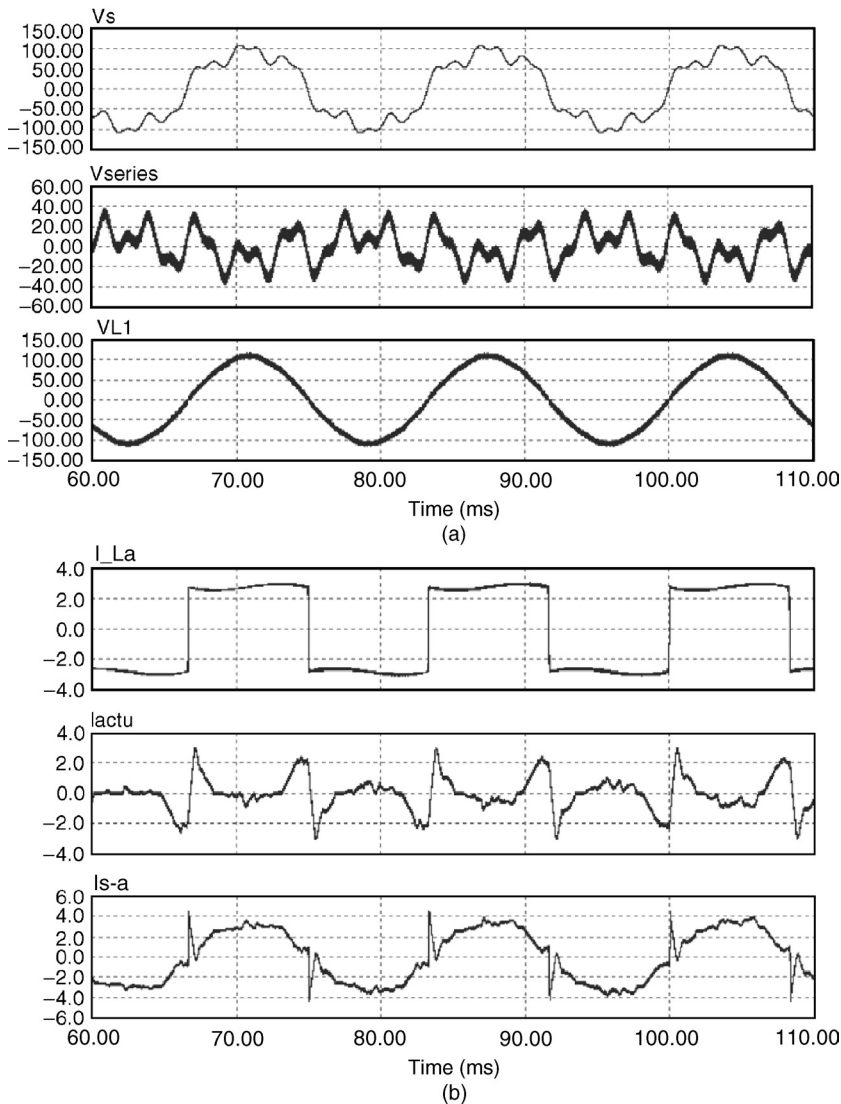
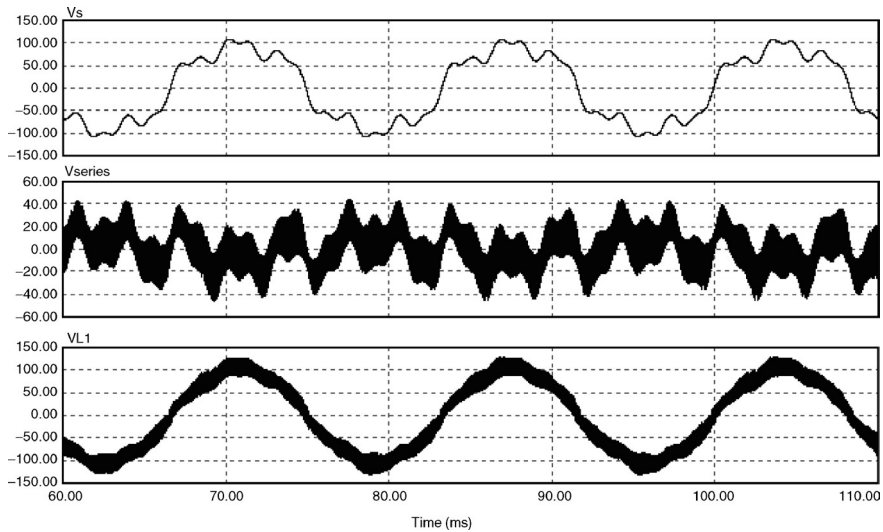


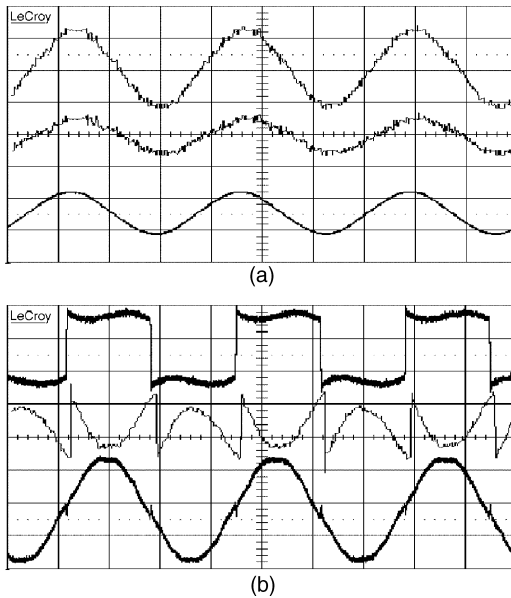
FIGURE 5.16 Simulation results of the three-leg UPQC: (a) line and load voltage, and (b) load and line current.

The main types of the static UPS systems are on-line, off-line, and line-interactive configurations. The main advantages of off-line UPS topology are a simple design, low cost, and small size. The line conditioning is passive and, hence, the technique is very robust. Disadvantages include: no output voltage regulation, long switching time, and poor performance with nonlinear loads.

Although, the on-line UPS system is widely recognized as a superior topology in performance, power conditioning, and load protection; the low

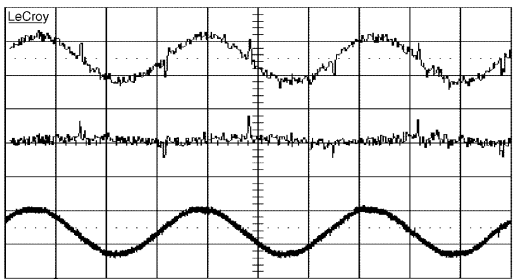
**FIGURE 5.17**

Simulation results of the three-leg UPQC with the second function, line and load voltage.

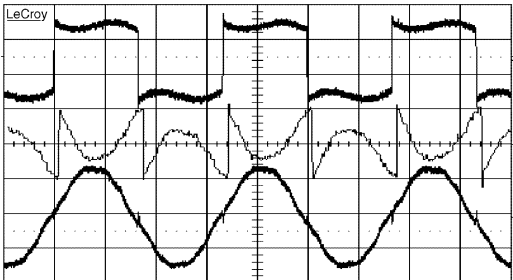
**FIGURE 5.18**

Experimental results of the full-bridge UPQC in the presence of voltage swell and voltage and current harmonics: (a) voltage of line, load, and UPQC, and (b) current of load, line, and UPQC.

efficiency is inherent to this topology due to the double-conversion nature of this UPS. Power flow through the rectifier and inverter during the normal operation means higher power losses and lower efficiency compared to off-line and line-interactive UPS systems.

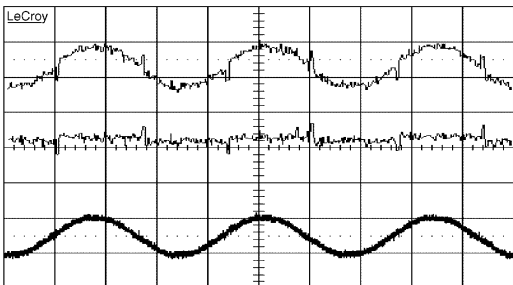


(a)

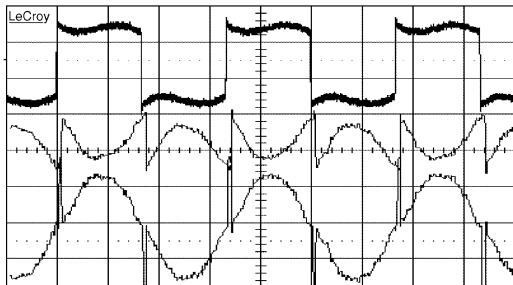


(b)

FIGURE 5.19
Experimental results of the half-bridge UPQC in the presence of voltage and current harmonics: (a) voltage of line, load, and UPQC, and (b) current of load, line, and UPQC.



(a)



(b)

FIGURE 5.20
Experimental results of the three-leg UPQC in the presence of voltage and current harmonics: (a) voltage of line, load, and UPQC, and (b) current of load, line, and UPQC.

Line-interactive UPS systems, with their simple design, high reliability, and lower cost provide an attractive alternative to the on-line UPS systems. Since this is a single-stage conversion topology, the efficiency is inherently higher than that of the double-conversion UPS. The main disadvantage is

the fact that the output voltage conditioning is not as good as that in on-line UPS systems because the inverter is not connected in series with the load.

The new series-parallel line-interactive UPS topology combines the advantages of both on-line and line-interactive UPS systems. It can simultaneously achieve unity power factor, precise regulation of the output voltage, and high efficiency. Its configuration is shown in Figure 5.21.

It consists of two bidirectional converters connected back to back, a common battery set, a static switch, and a series transformer. The front-end converter is connected with a series transformer to the main AC line. It is rated at about 20% of the output power of the whole system. The back-end converter is connected in parallel with the load and, in fact, is the conventional inverter for a line-interactive UPS system. It is rated at 100% of the output power. The main function of the back-end converter is to keep the output voltage stable at the rated nominal value. It also regulates the input power factor to unity and, at the same time, controls the charging of the battery. The front-end converter is in charge of compensating any unbalance between the output and input voltages.

The UPS system has two operating modes: normal mode and stored-energy mode. During the normal mode of operation, when the AC line is within the preset tolerance, most of the power is supplied directly from the AC line to the load. Only a small portion of the total power, usually less than 20%, flows through both the series and parallel converters. This power is needed to compensate for any difference between the input and output voltages and for power factor correction. At the same time, the parallel inverter charges the battery bank.

During the stored-energy mode of operation, when the input voltage is beyond a preset tolerance, the static switch trips off the main AC power supply and the back-end converter draws power from the battery bank acting as a conventional DC/AC inverter supplying the load with uninterrupted power.

Since an important portion of the consumed power flows without any conversion from the AC line to the load, the overall efficiency is higher than that of an on-line UPS system. At the same time, it provides excellent power conditioning and simultaneously achieves unity input power factor. This

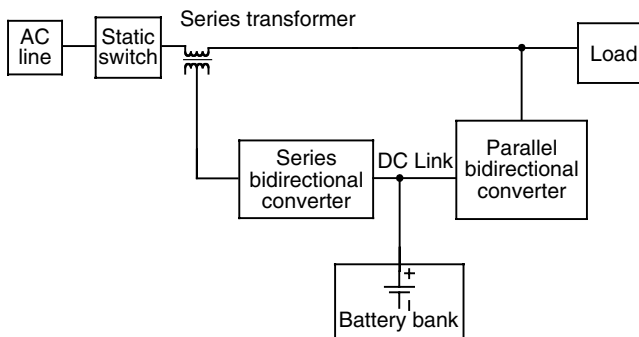


FIGURE 5.21

Block diagram of a typical series-parallel line-interactive UPS.

way eliminates the main drawback of the on-line UPS systems without compromising the performance, and as a result the series-parallel UPS topology appears to be a strong competitor of on-line UPS systems in many applications and has been attracting the attention of many researchers recently. However, not much work has been focused on applying different converter topologies, and especially converters with reduced number of switches, to the concept of series-parallel UPS systems. In this chapter, we present two reduced-parts single-phase series-parallel UPS topology, and explain their control strategies and operational principles in detail. Simulation and experimental results are presented to help understand the theoretical description of the systems.

5.3.1 Single-Phase Configuration Based on Two Full-Bridge Bidirectional Converters

A conventional series-parallel UPS topology consists of two full-bridge bidirectional converters connected to a common DC-link bus. A series-parallel UPS topology based on two full-bridge bidirectional converters is shown in Figure 5.22.

The series bidirectional converter consists of four switches and is rated at about 20% of the output power of the UPS system. It is connected via a transformer in series with the AC line. The parallel bidirectional converter consists of four switches and is rated at 100% of the output power. Different operating modes of the system are discussed below.

5.3.1.1 Bypass Mode

This mode of UPS system is the same as the first functionality of the UPQC system mentioned in Section 5.2.2.1. In this mode, the input voltage is in the range of 20% of its nominal value. The series converter compensates the

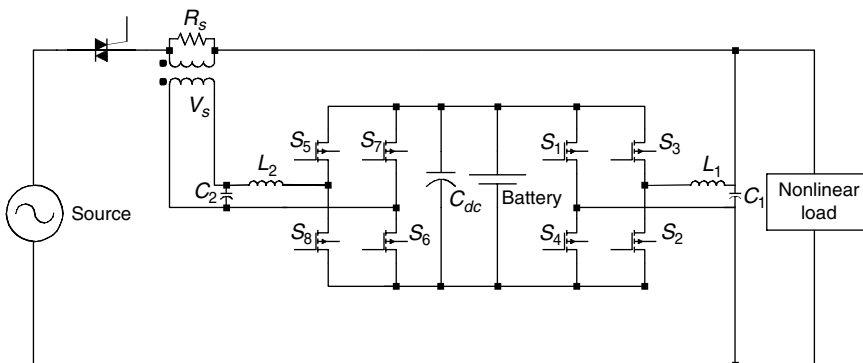


FIGURE 5.22

A series-parallel UPS topology based on two full-bridge bidirectional converters.

voltage difference of the input and reference voltage and regulates the voltage of load terminal. This converter has the ability to cancel any voltage disturbance such as harmonics, voltage sags and swells, and spikes. It gives or absorbs active power in the case of voltage sags and swells, respectively. For compensating the voltage harmonic of the source side, it only delivers reactive power.

In this mode, the parallel inverter accomplishes three functions simultaneously. It compensates the current harmonics produced by the load. At the same time, it compensates the reactive current drawn by the load and improves the power factor of the system. On the other hand, it draws a small component of fundamental current to recharge the DC-link battery. The equivalent circuit of the system in the bypass mode is the same as in Figure 5.23.

5.3.1.1.1 Voltage Control

Similarly, a PLL is used to produce the reference voltage. The input of PLL is the line voltage. The output of PLL is a 60 Hz reference voltage, which is in phase with the line voltage with negligible delay. Figure 5.24 shows the block diagram of the voltage control of the series converter.

The transfer function from reference voltage to output current is as follows. Figure 5.25 shows the frequency response of the series converter. The bandwidth of the transfer function is about 12,000 rad/sec, which is more than the frequency range of voltage disturbances in the power system.

$$\frac{V_s}{V_{ref}} = \frac{[K_p R_s C_2 s^2 + (K_I R_s C_2 + K_p) + K_I]}{L_2 C_2 s^3 + (K_p R_s C_2 + R_s C_2) s^2 + [(K_p + K_I R_s C_2) + 1] s + K_I} \quad (5.8)$$

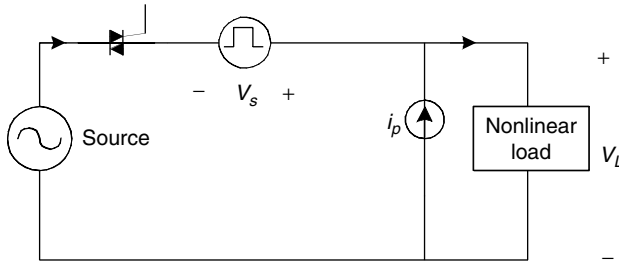


FIGURE 5.23
Equivalent circuit of the system in the bypass mode.

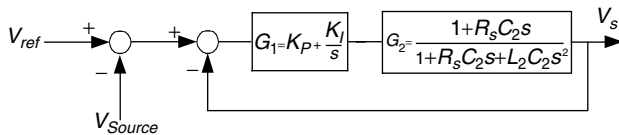
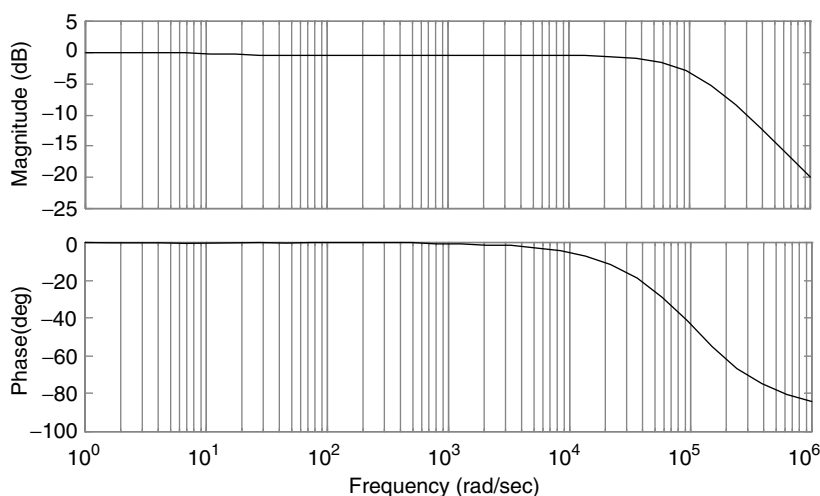


FIGURE 5.24
Block diagram of voltage control of the series converter.

**FIGURE 5.25**

Frequency response of the series converter.

5.3.1.1.2 Current Control

The same block diagram as the UPQC system is used to control the current of parallel converter. The only difference is that a large component of active current is drawn from the power system to charge the battery pack.

The transfer function of current of the parallel converter to reference current is as follows:

$$\frac{i_f}{i_f^*} = \frac{K_p s + K_I}{L_2 s^2 + K_p s + K_I} \quad (5.9)$$

For the storage systems, state of charge (SOC) of the battery should be considered. Although the battery has to be recharged when there is a voltage swell; but for the proper operation of the system during disturbances, the battery must be fully charged at all times. The SOC of the battery can be calculated using voltage, current, and temperature sensors. Usually, the battery of a UPS system consists of 120 lead–acid battery cells with a nominal voltage of 2 V. The discharge voltage level for this type of battery is considered 1.75 V or 87.5% of the nominal voltage. When the battery is fully charged, there is no need to draw active current from the source by a parallel converter. The same PI controller is also used to control the voltage of the DC-link.

5.3.1.2 Backup Mode

When the difference between the input voltage and reference voltage exceeds a specific range, which is determined by the rating of the series converter, the static switch isolates the source, and the parallel converter supplies the load. The voltage of the terminal of the parallel converter, which is

the voltage of the load terminal, is regulated by the series converter. After isolation of the source, the parallel converter drops all of its controlling functions and supplies the load by the sinusoidal voltage. The reference voltage is the output of PLL, which is freewheeling at 60 Hz.

When the source voltage recovers, the PLL synchronizes itself with the line voltage. After completion of synchronization, the static switch connects the line, and the series converter starts regulating. Figure 5.26 shows the block diagram of voltage control of the parallel converter in the backup mode.

5.3.2 Single-Phase Configuration Based on Two Half-Bridge Bidirectional Converters

A UPS topology, based on two half-bridge bidirectional converters connected to a common DC-link, is a quite popular solution in cost-sensitive low-power on-line UPS systems. This AC/DC/AC converter topology has not been applied to the series-parallel UPS systems yet. The series bidirectional converter consists of two switches connected to a split DC bus, composed of two capacitors C_{dc1} and C_{dc2} . The parallel bidirectional converter consists of two switches. The reduced number of switches results in a price lower than that of a full-bridge based topology. It should be noted, however, that the voltage utilization is worse and the harmonics content of the output is higher. A series-parallel UPS topology based on two half-bridge bidirectional converters connected to a common DC-link bus is shown in Figure 5.27. The

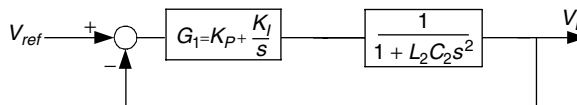


FIGURE 5.26
Block diagram of voltage control of the parallel converter.

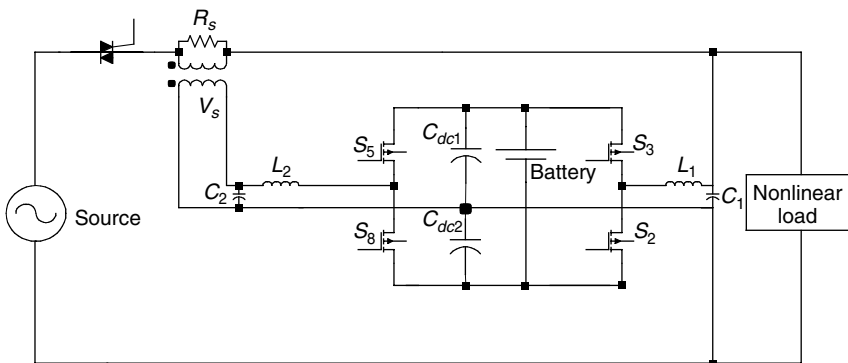


FIGURE 5.27
A half-bridge single-phase UPQC.

control strategy of this system is the same as the 4-leg converter. Figure 5.28 shows the simulation results of the system in the bypass mode.

5.3.3 Single-Phase Configuration Based on the Three-Leg Topology

The application of three-leg AC/DC/AC converter topology for a UPQC system was explained in Section 5.2.4. The same topology can be used for a UPS system. However, the three-leg AC/DC/AC converter has not been applied to the series-parallel UPS topology yet. A series-parallel UPS topology based on the three-leg UPS system is shown in [Figure 5.29](#).

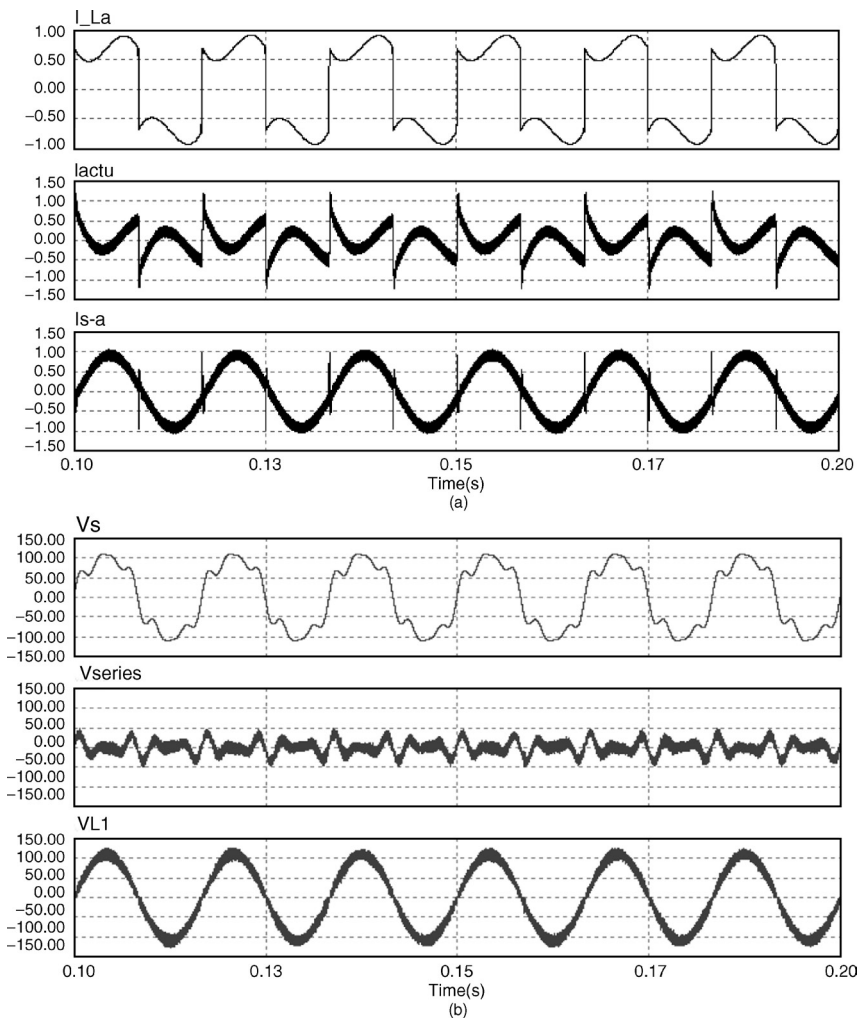
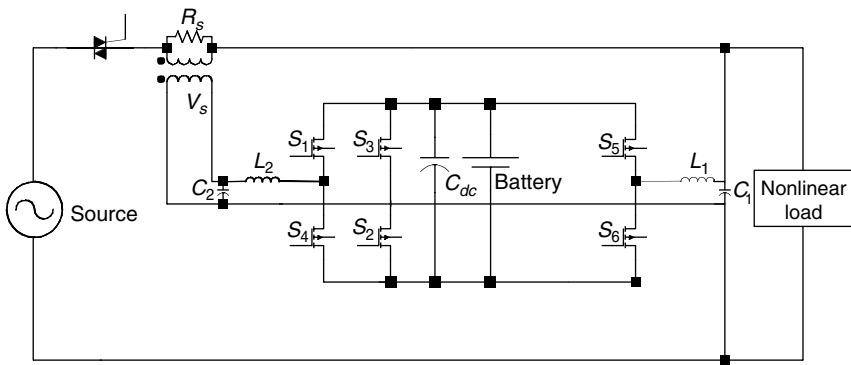


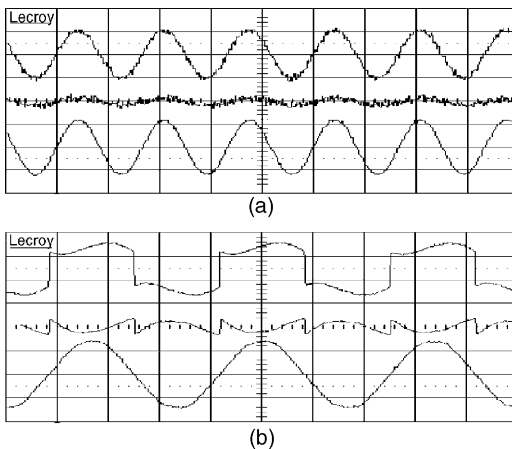
FIGURE 5.28 Simulation results of the half-bridge UPS system in bypass mode: (a) load and line current, and (b) line and load voltage.

**FIGURE 5.29**

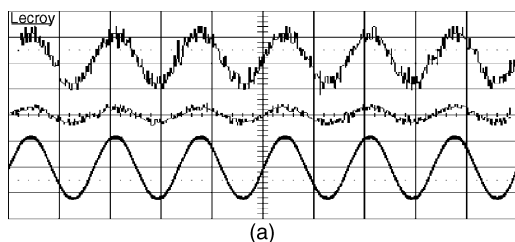
A series-parallel UPS topology based on two half-bridge bidirectional converters.

The series bidirectional converter consists of the first leg, switches S_1 and S_4 , and is rated at about 20% of the output power of the UPS system. The parallel bidirectional converter consists of the third leg—switches S_5 and S_6 , and is rated at 100% of the output power. The second leg, switches S_2 and S_3 , is common for both series and parallel converters. In the bypass mode, the series converter is considered as the main converter because the voltage regulation for the load is the first priority of the UPS system. The series converter regulates the line voltage and makes a sinusoidal voltage for the load. The operation of this converter is the same as the series converter in Sections 5.3.2 and 5.3.3. In this mode, the parallel converter has limitations. The operation of the parallel converter depends on the operation of the series converter. S_5 can be turned on when S_2 is on and S_6 can be turned on when S_3 is on.

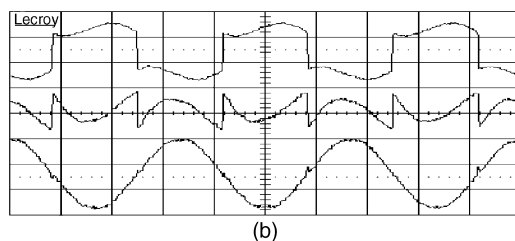
When the line voltage is beyond the predefined range, the static switch opens the line and the parallel converter supplies the load. The operation and performance of the system are the same as the system in Section 5.3.2.

**FIGURE 5.30**

Experimental results of the full-bridge UPS in the presence of voltage sag and voltage and current harmonics: (a) voltage of line, load and series converter, and (b) current of load, line, and parallel converter.



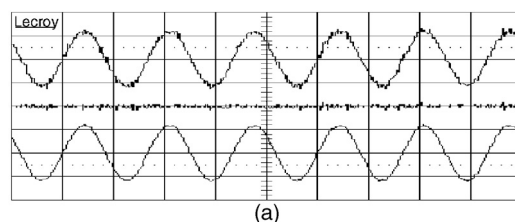
(a)



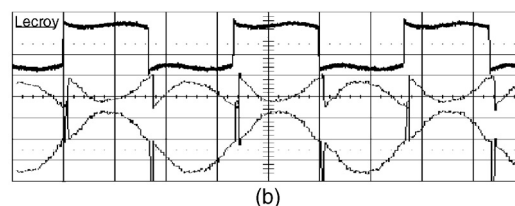
(b)

FIGURE 5.31

Experimental results of the half-bridge UPS in the presence of voltage and current harmonics: (a) voltage of line, load, and series converter, and (b) current of load, line, and parallel converter.



(a)



(b)

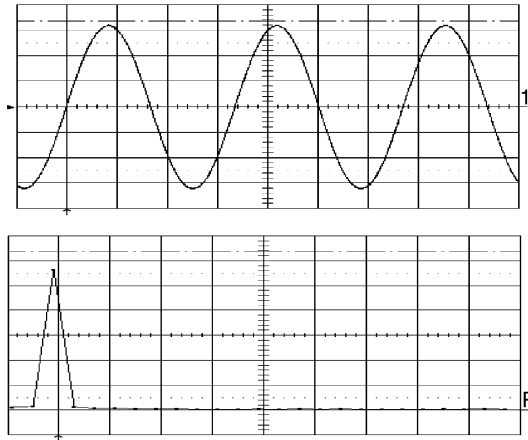
FIGURE 5.32

Experimental results of the three-leg UPS in the presence of voltage and current harmonics: (a) voltage of line, load, and series converter, and (b) current of load, line, and parallel converter.

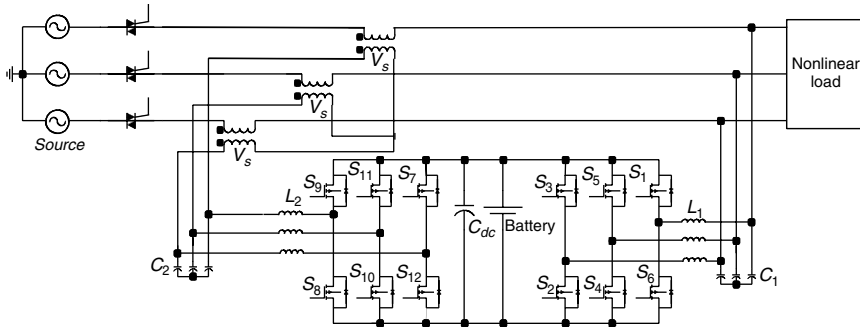
Typical experimental results for the line voltage sag compensation and the voltage and current harmonic cancellation for the full-bridge system are shown in Figure 5.30. Voltage sag compensation and voltage and current harmonic mitigations of a half-bridge system are shown in Figure 5.31. Voltage and current harmonic compensation of the three-leg system are shown in Figure 5.32. The voltage of the load terminal in the backup mode of a full-bridge UPS system is shown in Figure 5.33.

5.4 Reduced-Parts Three-Phase Series-Parallel Configurations

A conventional series-parallel three-phase UPS topology consists of two full-bridge bidirectional converters connected to a common DC-link bus. A

**FIGURE 5.33**

Full-bridge UPS: voltage of the load in the backup mode and its frequency spectrum.

**FIGURE 5.34**

A series-parallel UPS topology based on two three-leg bidirectional converters.

three-phase series-parallel UPS topology based on two full-bridge bidirectional converters is shown in [Figure 5.35](#). The series bidirectional converter consists of six switches and is rated at about 20% of the output power of the UPS system. It is connected via a transformer in series with the AC line. The parallel bidirectional converter consists of six switches, and is rated at 100% of the output power. A UPS topology, based on two 2-leg bidirectional converters connected to a common DC-link, is a cost-effective alternative to the topology shown in [Figure 5.34](#). This topology is shown in [Figure 5.35](#). The analysis of the converter in the backup and bypass modes is discussed in the following.

5.4.1 Bypass Mode

[Figure 5.36](#) shows the equivalent circuit of the system in the bypass mode. The series converter controls the output voltage. The parallel converter shapes the line current and improves the power quality. At the same time, it recharges the DC battery.

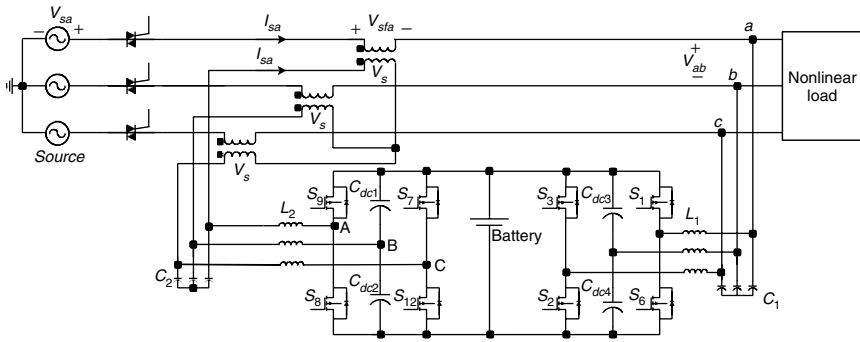


FIGURE 5.35

A series-parallel UPS topology based on two 2-leg bidirectional converters.

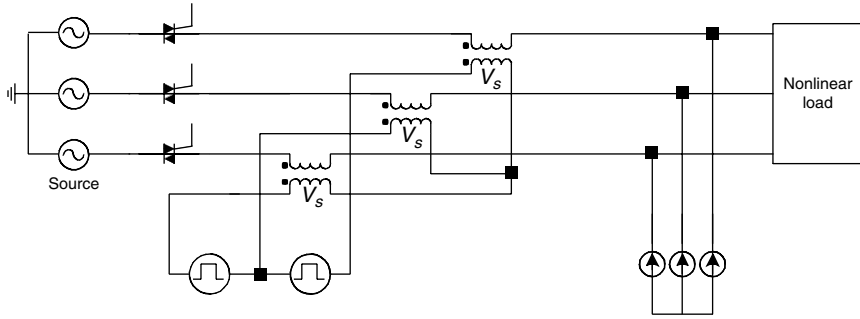


FIGURE 5.36

The equivalent circuit of the system in the bypass mode.

5.4.1.1 Voltage Control

In this topology, instead of controlling the phase voltage, the phase-to-phase voltage is controlled. The phasor diagram of the voltages in the presence of disturbance is shown in Figure 5.37. The voltage equations of the system are as follows:

$$(V_{sa} - V_{sfa}) - (V_{sb} - V_{sfb}) = V_{ab} \quad (5.10a)$$

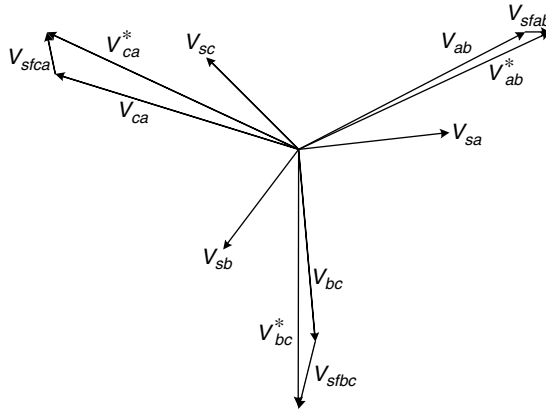
$$(V_{sc} - V_{sfc}) - (V_{sb} - V_{sfb}) = V_{cb} \quad (5.10b)$$

From Equations 5.9 and 5.10, we have

$$V_{sab} - (V_{sfa} - V_{sfb}) = V_{ab} \quad (5.11)$$

$$V_{scb} - (V_{sfc} - V_{sfb}) = V_{cb} \quad (5.12)$$

where $V_{sab} = V_{sa} - V_{sb}$, $V_{scb} = V_{sc} - V_{sb}$ and $V_{cb} = -V_{bs}$

**FIGURE 5.37**

Phasor diagram of the voltages of the system in the presence of disturbance.

$$V_{AB} = (i_{sa} - i_{sb})L_2s + (V_{sfa} - V_{sfb})L_2C_2S^2 + V_{sfab} \quad (5.13)$$

$$V_{AB} = (i_{sa} - i_{sb})L_2s + V_{sfab}L_2C_2S^2 + V_{sfab} \quad (5.14)$$

As shown in Equations 5.6 and 5.7, the line voltages, V_{ab} and V_{bc} , can be controlled by controlling V_{sfab} and V_{sfb} . V_{sfab} and V_{sfb} are controlled by the output of the PWM, V_{AB} . Figure 5.38 shows the block diagram of the voltage control of the series converter and its frequency response. The same controller is used for V_{sfb} . The relation between the line voltages is as follows:

$$V_{ab} + V_{bc} + V_{ca} = 0 \quad (5.15)$$

Based on Equation 5.15, by controlling and regulating V_{ab} and V_{bc} , V_{ca} is automatically controlled. As shown in Figure 5.43, the reference voltages for V_{ab} and V_{bc} are as follows:

$$V_{ab}^* = \sqrt{3}V_{sa}^* \sin(\omega t + 30) \quad (5.16)$$

$$V_{bc}^* = \sqrt{3}V_{sb}^* \sin(\omega t + 30) \quad (5.17)$$

Considering the line current difference, $i_{sa} - i_{sb}$, as disturbance, the transfer function of V_{sfab}/V_{sfab}^* is as follows:

$$\frac{V_{sfab}}{V_{sfab}^*} = \frac{K_p s + K_I}{L_2 C_2 S^3 + (K_p s + 1)s + K_I} \quad (5.18)$$

The bandwidth of the transfer function is about 20,000 rad/sec. This bandwidth covers most of the voltage disturbances that occur in the power system.

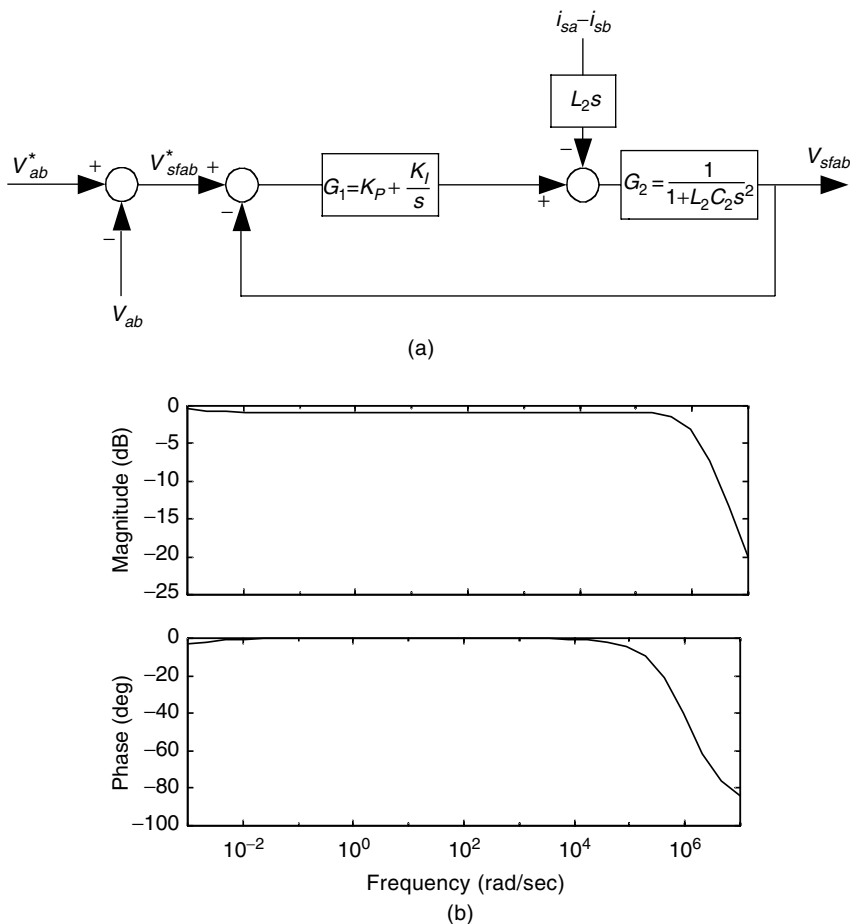


FIGURE 5.38

Series converter: (a) block diagram of voltage control, and (b) frequency response.

5.4.1.2 Current Control

The three-phase synchronous reference frame method is used for the current control of this converter as well. The relation between the line currents of the system is as follows:

$$i_a + i_b + i_c = 0 \quad (5.19)$$

Based on Equation 5.14, by controlling and regulating i_a and i_c , i_b is automatically controlled. Figure 5.39 shows the block diagram of the current controller for phases a and c . The transfer function of i_f/i_f^* is as follows:

$$\frac{i_f}{i_f^*} = \frac{K_P s + K_I}{L_1 s^2 + K_P s + K_I} \quad (5.20)$$

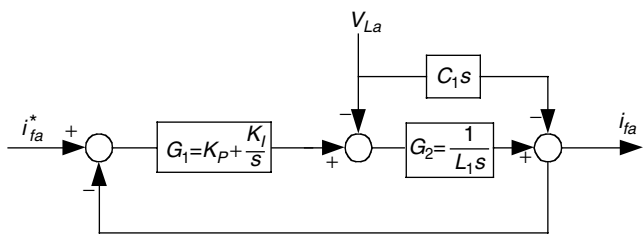


FIGURE 5.39
Block diagram of the current control of a parallel converter in the bypass mode.

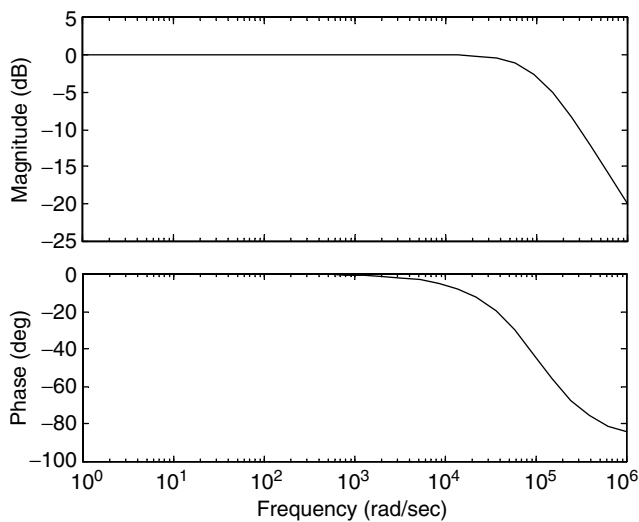


FIGURE 5.40
Frequency response of the parallel converter.

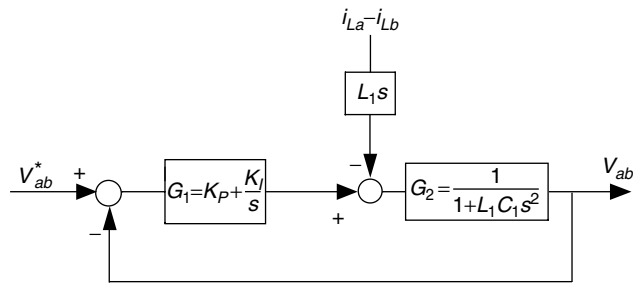
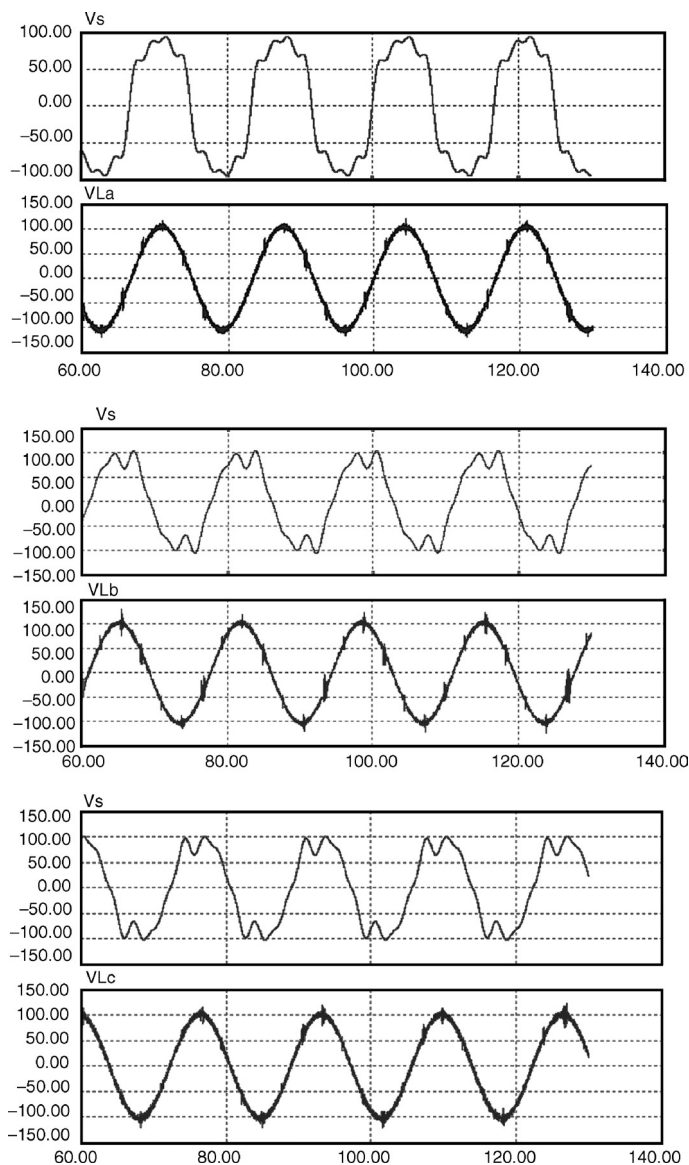
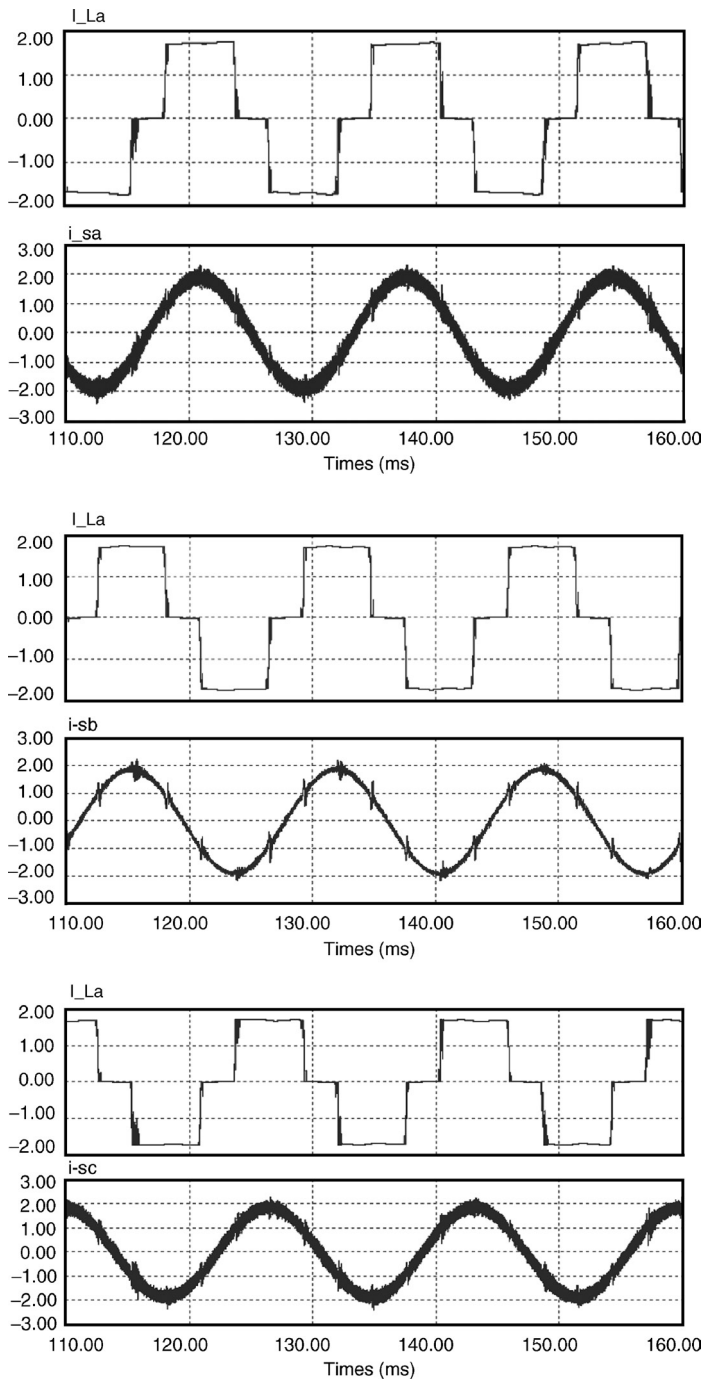


FIGURE 5.41
Block diagram of the voltage control of the parallel converter in backup mode.

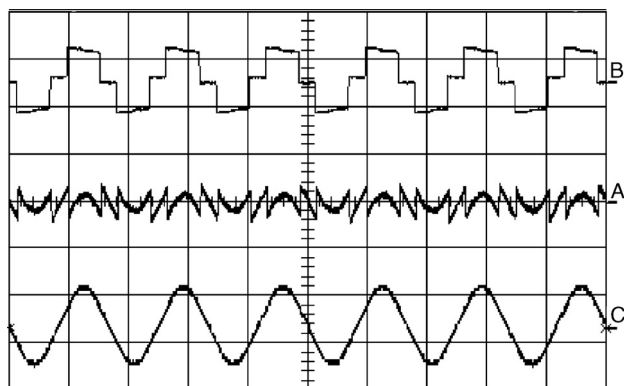
**FIGURE 5.42**

Simulation result for the three phases of the series converter in the presence of voltage sag and harmonics.

The frequency response of the parallel converter is shown in [Figure 5.40](#). The bandwidth is mostly affected by L_1 . The bandwidth increases when the inductor decreases. On the other hand, when the inductor decreases, current harmonics with switching frequency appear in the line current. Therefore, an appropriate value must be chosen for this inductor.

**FIGURE 5.43**

Simulation results of current of three phases of the parallel converter.

**FIGURE 5.44**

Experimental results of one phase of the parallel converter, from top to bottom: current of load, parallel converter, and line.

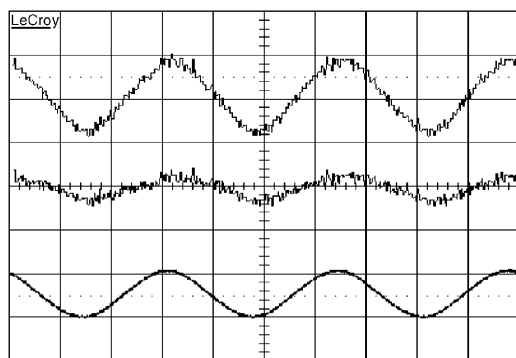
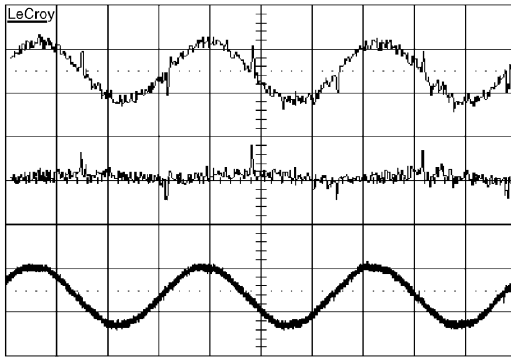


FIGURE 5.45 Experimental results of series converter for voltage swell compensation, from top to bottom: voltage of line, series converter, and load (X-axis 5 mS/div, Y-axis 200 V/div).

5.4.2 Backup Mode

When the difference between the input voltage and reference voltage exceeds the specific range, which is determined by the rating of the series converter, the static switch isolates the source, and the parallel converter supplies the load. The terminal voltage of the parallel converter, which is the voltage of the load terminal, is regulated by the series converter. After isolation of the source, the parallel converter eliminates all its controlling functions and supplies the load by the sinusoidal voltage. The reference voltage is the output of the phase-to-phase PLL, which is freewheeling at 60 Hz.

As explained in the series converter voltage control section, Equations 5.15 through 5.18, the line voltages V_{ab} and V_{bc} are controlled. The reference voltage for line voltage is as in Equations 5.20 and 5.21. Based on Equation 5.15, V_{ca} is controlled automatically. A block diagram of the voltage control of the parallel converter in the backup mode is shown in [Figure 5.41](#). Considering

**FIGURE 5.46**

Experimental results of series converter for voltage harmonic compensation, from top to bottom: voltage of line, series converter, and load (X-axis 5 mS/div, Y-axis 200 V/div).

TABLE 5.3

Parameters of the circuit

P_{Load}	C_{dc}	L_1	C_1	L_2	C_2
1300 W	1360 μF	1 mH	4.7 μF	0.1 mH	2.7 μF

the difference of the load current as a disturbance, the transfer function of V_{ab}/V_{ab}^* is as follows:

$$\frac{V_{ab}}{V_{ab}^*} = \frac{K_p s + K_I}{L_2 C_1 s^3 + (K_p + 1)s + K_I} \quad (5.21)$$

When the source voltage recovers, the PLL synchronizes itself with the line voltage. After completion of the synchronization, the static switch connects the line, and the series converter starts regulating. Figure 5.42 and Figure 5.43 show the simulation results of the system in the bypass mode. Voltage and current of phase *b* are a function of voltage and current of phases *a* and *c*. Therefore, its waveforms are different.

The typical experimental results of a system using a TMS320LF2407 digital signal processor (DSP) are shown in Figure 5.44, Figure 5.45, and Figure 5.46. The parameters of the system are shown in Table 5.3. The voltage of the DC bus is 440 V. The current of phase *a* of load, parallel converter, and line are shown in Figure 5.44. Voltages of the line series converter and the load are shown in Figure 5.45 and Figure 5.46. The parallel converter regulates the line current and the series converter regulates the load voltage.

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6

Modeling, Analysis, and Digital Control

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As discussed in previous chapters, active filters have been known as one of the best tools for harmonic mitigation as well as reactive power compensation, load balancing, voltage regulation, and voltage flicker compensation. Active filters have been designed, improved, and commercialized in the last 25 years. They are applicable for the compensation of current-based distortions such as current harmonics, reactive power, and neutral current. They are also used for voltage-based distortions such as voltage harmonics, voltage flickers, voltage sags and swells, and voltage unbalances. In this chapter, modeling and analysis of active filter systems using the generalized state space averaging method are explained. Additionally, digital control of active filters and series-parallel uninterruptible power supplies is discussed.

6.1 Systems Modeling Using the Generalized State Space Averaging Method

Since its inception, very few studies have been done on modeling and analysis of active filters. In fact, most of the works have been on modeling of the control systems and operating principles of active filters. Simulation and analysis of active filters have been done by computational and modeling software packages such as MATLAB, PSpice, Saber, and PSIM. Actual elements such as switches and passive components are used for simulating active filter systems. In this case, nonlinearity of real elements causes many problems such as long execution time, divergence, and large produced files.

Recently, some works have been done on modeling of electrical systems based on the switching functions method [1, 2] and the generalized state space averaging method [3–5]. This research has shown the ability of these methods for modeling and analysis of power electronic circuits. Several references have also studied the stability assessment of systems modeled with the generalized state space averaging method [6, 7]. This method is derived from Fourier transform for nonperiodic signals. Using this method, the nonlinearity of the system is eliminated. The relation between the state variables of the system is expressed by linear equations. An exact and fast approximation of the system parameters is achieved. The problems of long execution time, divergence, and large output files mentioned no longer exist. Additionally, frequency decomposition of all parameters of the system is done and their harmonic spectra are achieved.

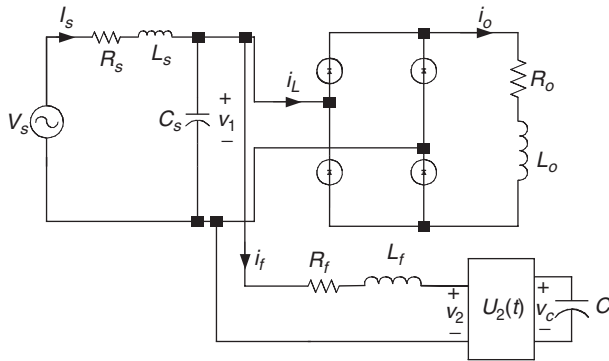
6.1.1 Fundamental Equations

For simplicity of analysis, first we consider a shunt single-phase voltage source active filter. The typical topology of this active filter is shown in Figure 6.1. R_s and L_s are the resistance and inductance of the source side. C_s is the equivalent capacitor of the power network. This capacitor with the link inductor between the active filter and system, L_p , shape a second-order passive filter to cancel the switching frequency of the active filter. If the value of this capacitor is not sufficient, additional capacitance must be added to the system. The inductance of the load is considered large enough to maintain the load current continuous.

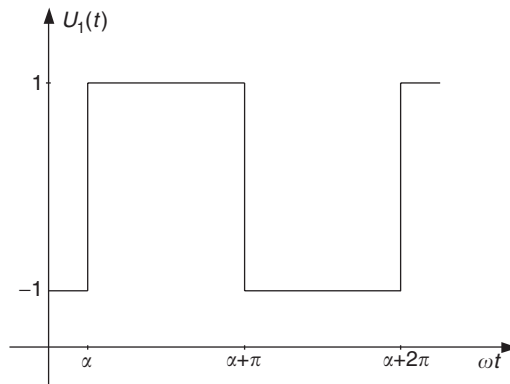
We consider two switching functions for the load rectifier and active filter inverter. With these two switching functions, we define an analytic function instead of the actual switches. Input and output relations of the AC/DC converter can simply be expressed using $u_1(t)$ depicted in Figure 6.2, as follows:

$$i_L = i_o u_1(t) \quad (6.1)$$

$$V_o = V_1 u_1(t) \quad (6.2)$$

**FIGURE 6.1**

Topology of a typical active filter system.

**FIGURE 6.2**

Switching function of the AC/DC rectifier.

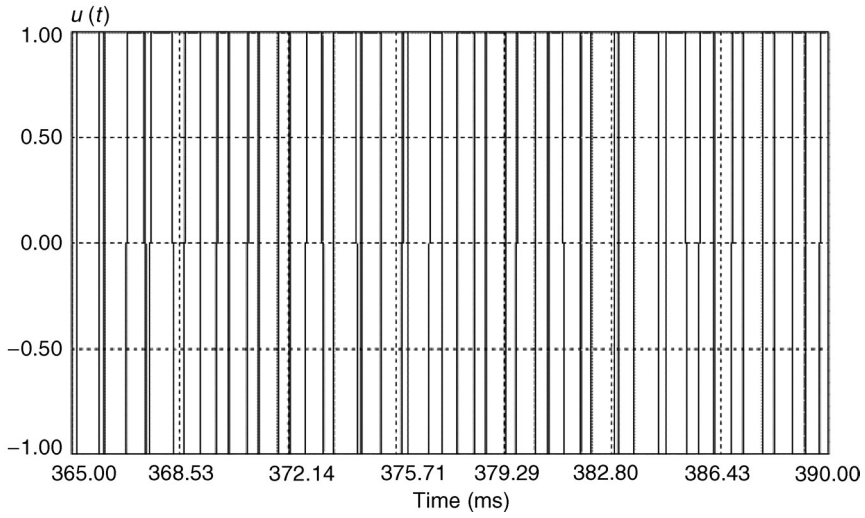
The relation of input and output voltage and current of the active filter can be expressed using a more complicated switching function. This function is depicted in [Figure 6.3](#). The relationship between the parameters of the active filter is as follows:

$$i_C = -i_F u_2(t) \quad (6.3)$$

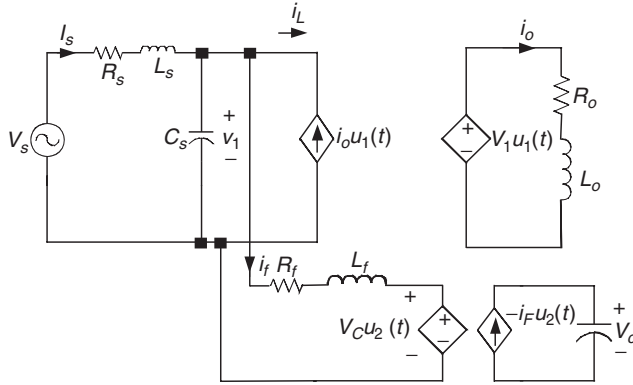
$$V_2 = V_C u_2(t) \quad (6.4)$$

Using these two switching functions, our proposed topology is converted to the topology illustrated in [Figure 6.4](#) in terms of passive elements, dependent voltage, and current sources. Now, we can write the state equations of the system as follows:

$$\frac{di_o}{dt} = \frac{1}{L_o} [v_1 u_1(t) - R_o i_o] \quad (6.5)$$

**FIGURE 6.3**

Switching function of the active filter.

**FIGURE 6.4**

The converted topology of the active filter system.

$$\frac{dv_c}{dt} = -\frac{1}{C} i_f u_2(t) \quad (6.6)$$

$$\frac{di_s}{dt} = \frac{1}{L_s} [v_s - v_1 - R_s i_s] \quad (6.7)$$

$$\frac{di_f}{dt} = \frac{1}{L_f} [v_1 - v_c u_2(t) - R_f i_f] \quad (6.8)$$

$$\frac{dv_1}{dt} = \frac{1}{C_s} [i_s - i_f - i_o u_1(t)] \quad (6.9)$$

where $u_1(t)$ is the switching function of the AC/DC-controlled rectifier and is shown in Figure 6.2. $u_2(t)$ is the switching function of the active filter and is shown in Figure 6.3.

6.1.2 Generalized State Space Averaging Method

The generalized state space averaging method is derived from Fourier transform for nonperiodic signals. In fact, each signal, $x(t)$, can be approximated with finite coefficients of Fourier transform in a finite time interval. The precision of the estimation can be increased by considering more coefficients [5, 6]. Fourier transform of a signal, $x(t)$, in the time interval of $[t-T, t]$ is as follows:

$$x(t) = \sum_{k=-n}^n \langle x \rangle_k(t) e^{jk\omega t} \quad (6.10)$$

where

$$\omega = \frac{2\pi}{T}, \quad \langle x \rangle_k(t) = \frac{1}{T} \int_{t-T}^t x(\tau) e^{-jk\omega \tau} d\tau \quad (6.11)$$

In Equation 6.10, the value of n depends on the required accuracy, and if n approaches infinity, the approximation error approaches zero. If we only consider the term with $k=0$, we have the same state space averaging method [5]. However, the more terms we consider, the more accuracy we have.

The terms $\langle x \rangle_k(t)$ are complex Fourier coefficients. These coefficients are functions of time since the interval under the consideration slides as a function of time. The analysis computes the time-evolution of these Fourier transform coefficients as the window of length T slides over the actual waveform. Our approach is to determine an appropriate state space model in which the coefficients in Equation 6.11 are the state variables. Certain properties of the Fourier transform coefficients, which we need for our analysis, such as differentiation vs. time and transforms of multiplication of variables, are expressed as follows:

$$\frac{d}{dt} \langle x \rangle_k(t) = -jk\omega \langle x \rangle_k(t) + \left\langle \frac{d}{dt} x \right\rangle_k(t) \quad (6.12)$$

$$\langle x \cdot y \rangle_k = \sum_i \langle x \rangle_i \langle y \rangle_{k-i} \quad (6.13)$$

6.1.3 Modeling of Single-Phase Active Filter System

For simplicity, we consider only the DC value of the output current, i_o , and voltage of the energy storage capacitor, v_c , in Figure 6.1. While we consider the value of the energy storage capacitor and the load inductance to be fairly large, these suggestions are reasonable.

$$\langle i_o \rangle_0 = x_1 \quad (6.14)$$

$$\langle v_c \rangle_0 = x_2 \quad (6.15)$$

For source current, i_s , we only consider the fundamental frequency. The other coefficients such as numbers 3, 5, and 7 show the residue harmonics in the source current, which do not affect our analysis directly.

$$\langle i_s \rangle_1 = x_3 + jx_4, \langle i_s \rangle_{-1} = x_3 - jx_4 \quad (6.16)$$

For the current of active filter, i_f , we consider the fundamental frequency and harmonics of orders three, five, and seven, which are the dominant current harmonics.

$$\langle i_f \rangle_1 = x_5 + jx_6, \langle i_f \rangle_{-1} = x_5 - jx_6 \quad (6.17)$$

$$\langle i_f \rangle_3 = x_7 + jx_8, \langle i_f \rangle_{-3} = x_7 - jx_8 \quad (6.18)$$

$$\langle i_f \rangle_5 = x_9 + jx_{10}, \langle i_f \rangle_{-5} = x_9 - jx_{10} \quad (6.19)$$

$$\langle i_f \rangle_7 = x_{11} + jx_{12}, \langle i_f \rangle_{-7} = x_{11} - jx_{12} \quad (6.20)$$

By considering the impedance of source side reasonable, we can suggest first harmonic approximation for v_1 .

$$\langle v_1 \rangle_1 = x_{13} + x_{14}, \langle v_1 \rangle_{-1} = x_{13} - x_{14} \quad (6.21)$$

For continuation of our analysis, we need the following derivations. The coefficients for $u_2(t)$ can be easily calculated by a simple computer program. We will have different values for different switching schemes. In fact, we can study the effects of different switching schemes on each harmonic component analytically. In other words, the study of any harmonic component can be done separately. This is one of the advantages of this method.

$$\langle u_1(t) \rangle_0 = 0, \langle u_1(t) \rangle_1 = \frac{-j^2}{\pi} \quad (6.22)$$

$$\langle v_s \rangle_1 = \frac{-jv_s}{2} \quad (6.23)$$

$$\langle u_2(t) \rangle_1 = 0.002 + j0.1467 \quad (6.24)$$

$$\langle u_2(t) \rangle_3 = 0.082 - j0.0132 \quad (6.25)$$

$$\langle u_2(t) \rangle_5 = 0.071 - j0.039 \quad (6.26)$$

$$\langle u_2(t) \rangle_7 = 0.055 - j0.053 \quad (6.27)$$

By applying time derivation and multiplication property into Equations 6.12 and 6.13, and by substituting Equations 6.14 through 6.21 into Equations 6.1 through 6.5 and considering Equations 6.22 through 6.27, the generalized

state space averaged model of the complete system for zero firing angle of the rectifier can be written as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \\ \dot{x}_5 \\ \dot{x}_6 \\ \dot{x}_7 \\ \dot{x}_8 \\ \dot{x}_9 \\ \dot{x}_{10} \\ \dot{x}_{11} \\ \dot{x}_{12} \\ \dot{x}_{13} \\ \dot{x}_{14} \end{bmatrix} = \begin{bmatrix} -\frac{R_o}{L_o} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{4}{\pi L_o} \\ 0 & 0 & 0 & 0 & \frac{0.004}{C} & \frac{0.2934}{C} & -\frac{0.164}{C} & \frac{0.0264}{C} & -\frac{0.0142}{C} & \frac{0.078}{C} & -\frac{0.11}{C} & \frac{0.106}{C} & 0 & 0 \\ 0 & 0 & -\frac{R_s}{L_s} & \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_s} & 0 \\ 0 & 0 & -\omega & -\frac{R_s}{L_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_s} \\ 0 & \frac{0.002}{L_f} & 0 & 0 & -\frac{R_f}{L_f} & \omega & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_f} & 0 \\ 0 & \frac{0.1467}{L_f} & 0 & 0 & \omega & -\frac{R_f}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_f} & 0 \\ 0 & -\frac{0.082}{L_f} & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 3\omega & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{0.0132}{L_f} & 0 & 0 & 0 & 0 & -3\omega & -\frac{R_f}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{0.071}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 5\omega & 0 & 0 & 0 & 0 \\ 0 & \frac{0.039}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & -5\omega & -\frac{R_f}{L_f} & 0 & 0 & 0 & 0 \\ 0 & -\frac{0.055}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_f}{L_f} & 7\omega & 0 & 0 \\ 0 & \frac{0.053}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -7\omega & -\frac{R_f}{L_f} & 0 & 0 \\ 0 & 0 & \frac{1}{C_s} & 0 & -\frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \omega \\ \frac{2}{\pi C_s} & 0 & 0 & \frac{1}{C_s} & 0 & -\frac{1}{C_s} & 0 & 0 & 0 & 0 & 0 & 0 & -\omega & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ x_{10} \\ x_{11} \\ x_{12} \\ x_{13} \\ x_{14} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ -\frac{V_s}{2L_o} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (6.28)$$

This equation can be solved easily by a computer software like MATLAB. The circuit's parameters can be computed by substituting these variables into Equation 6.10. The results are as the follows:

$$i_o(t) = x_1 \quad (6.29)$$

$$v_c(t) = x_2 \quad (6.30)$$

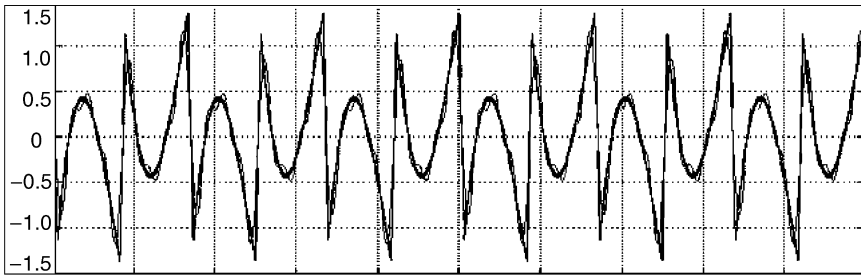
$$i_s(t) = 2x_3 \cos \omega t - 2x_4 \sin \omega t \quad (6.31)$$

$$\begin{aligned} i_f(t) = & 2x_5 \cos \omega t - 2x_6 \sin \omega t + 2x_7 \cos 3\omega t \\ & - 2x_8 \sin 3\omega t - 2x_9 \cos 5\omega t + 2x_{10} \sin 5\omega t \\ & - 2x_{11} \cos 7\omega t - 2x_{12} \sin 7\omega t \end{aligned} \quad (6.32)$$

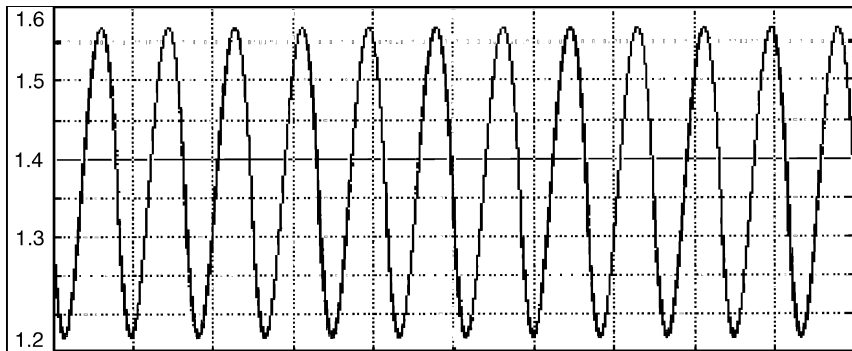
$$v_1(t) = 2x_{13} \cos \omega t - 2x_{14} \sin \omega t \quad (6.33)$$

6.1.4 Simulation Results

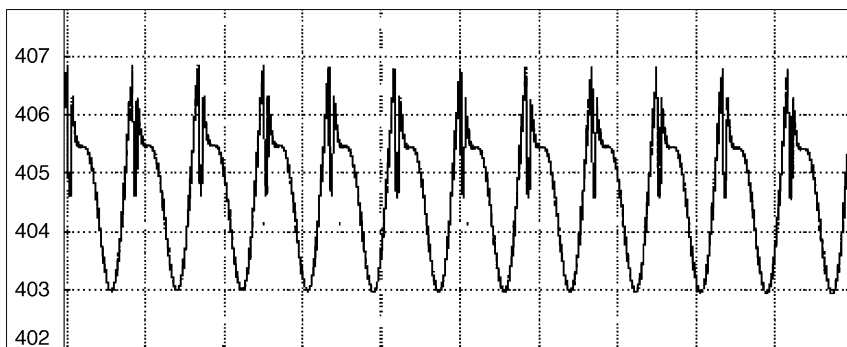
The circuit has been simulated using both the exact time-domain model and generalized model. The results are shown in [Figure 6.5](#), [Figure 6.6](#), and [Figure 6.7](#). Ordinary analysis is based on the topology. Simulating software

**FIGURE 6.5**

Current of the single-phase shunt active filter based on the actual method and generalized state space averaging (GSSA) method.

**FIGURE 6.6**

Load current (i_o) based on two methods.

**FIGURE 6.7**

Capacitor voltage (V_c) based on two methods.

packages such as PSpice, Saber, and PSIM, which use the actual model of switches, have some problems. The main problems are large produced files, long execution time, and, particularly, convergence problems. There are more problems associated with other types of software packages like

MATLAB, which uses transfer functions of the system for simulation. For this type of simulation device, all transfer functions for the system must be calculated. Calculation should be revised after every small change in the system. This is cumbersome and sometimes impossible.

In the proposed method, there is no need for the actual switch or even an approximation of the switch. By eliminating switches, the long execution time, divergence problem, and large produced files can be avoided. A very good and fast system approximation can be achieved. In addition, the decomposition of all parameters in the system is done, and their harmonic spectra are obtained. This method is applicable to all different topologies of active filters with different switching schemes.

6.1.5 Other Examples

The generalized state space averaging method is a general method and is applicable to any topology such as three-phase shunt active filters as well as single- and three-phase series active filters. Figure 6.8 shows a single-phase series active filter system. Two functions can be defined for this converter.

When the load is sensitive and critical, a series converter is used to regulate line voltage for the load. It cancels out any line voltage distortions such as voltage harmonics, sag, swell, and voltage unbalance. It is capable of eliminating any voltage harmonics with a frequency within the bandwidth of the control scheme. The second function of the series active filter, which is mostly considered in very high-power applications, is defined to protect the power system against the voltage distortions originating from the load. Some nonlinear loads, which usually have a capacitor bank after the bridge rectifier, appear to be voltage harmonic generators. The voltage harmonics at the point of common coupling affect the other sensitive loads connected to this point. The first function of the series active filter is considered in this chapter. The filter is used to compensate voltage harmonics of the input source. We again define two switching functions for this system. The state equations of the system are as follows:

$$\frac{di_o}{dt} = \frac{1}{L_o} [(v_{PCC} + v_f)u_1(t) - v_o] \quad (6.34)$$

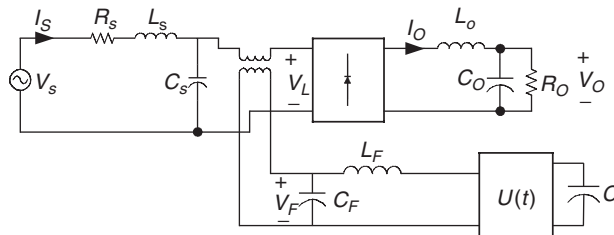


FIGURE 6.8

A typical topology of a series active filter.

$$\frac{dv_c}{dt} = -\frac{1}{C} i_f u_2(t) \quad (6.35)$$

$$\frac{di_s}{dt} = \frac{1}{L_s} [v_s - v_{PCC} - R_s i_s] \quad (6.36)$$

$$\frac{di_f}{dt} = \frac{1}{L_f} [v_c u_2(t) - v_f] \quad (6.37)$$

$$\frac{dv_{PCC}}{dt} = \frac{1}{C_{PCC}} [i_s - i_o u_1(t)] \quad (6.38)$$

$$\frac{dv_o}{dt} = \frac{1}{C_o} [i_o - \frac{v_o}{R}] \quad (6.39)$$

$$\frac{dv_f}{dt} = \frac{1}{C_f} [i_f - i_o - \frac{v_f}{R_f}] \quad (6.40)$$

The procedure of Section 6.1.4 has been done on this system with seven state variables. For the output voltage of the active filter, v_f , we consider the fundamental frequency and harmonics of orders three, five, and seven, which are suggested to be the dominant voltage harmonics of the source voltage. For other state variables, we consider either the fundamental frequency or the average DC value. The dimension of the resulting matrix is 17. The results of both the exact time-domain simulation and generalized state space averaging method are shown in [Figure 6.12](#), [Figure 6.13](#), [Figure 6.14](#), and [Figure 6.15](#). Figure 6.9 shows a three-phase shunt active filter system. Line harmonic cancellation and reactive current compensation are the main objectives of this converter. For this system, six switching functions and 11 state variables are defined.

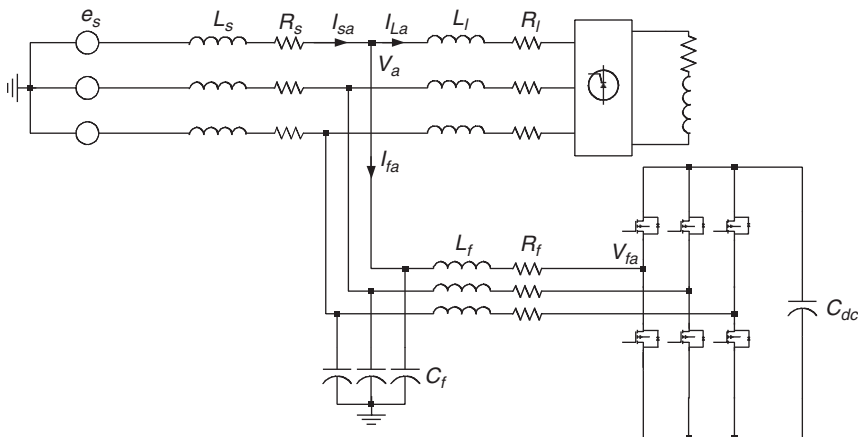


FIGURE 6.9

A typical three-phase shunt active filter.

In a balanced system, these switching functions are originally three functions with a 120° phase shift. The switching function of the three-phase load side AC/DC converter is shown in Figure 6.10. By defining the two main functions and disregarding load-side inductance, this system can easily be modeled and analyzed by the generalized state space averaging method. The converted topology is shown in Figure 6.11.

In this system, the number of equations is high and the final matrix is large; but due to the symmetry of the system, the equations and matrix are easily acquirable. Simulation results for this system are shown in Figure 6.16, Figure 6.17, Figure 6.18, and Figure 6.19.

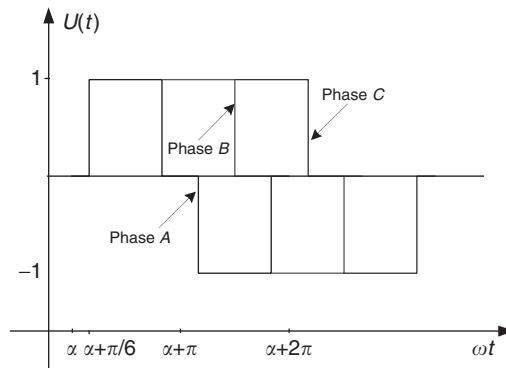


FIGURE 6.10

Switching function of three phases of an AC/DC converter.

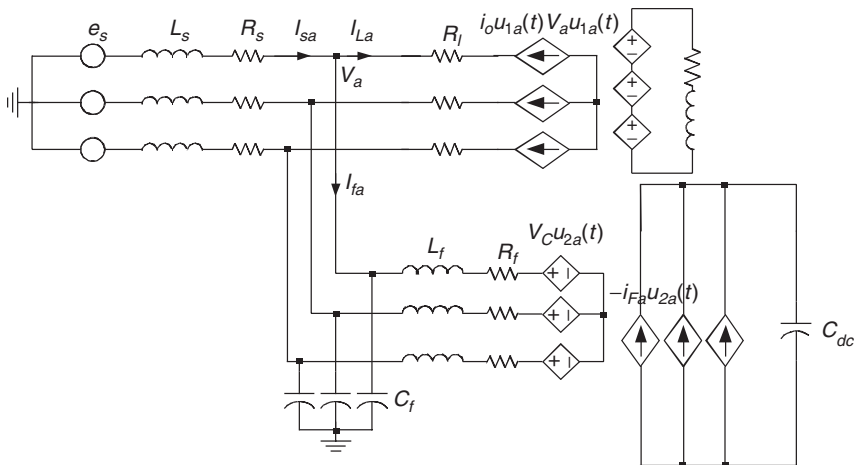


FIGURE 6.11

The converted topology of the three-phase shunt active filter.

Typical experimental results of a 1300 W system for the three-phase shunt active filter and a 650 W setup for the single phase shunt and series active filter systems are shown in Figure 6.20, Figure 6.21, and Figure 6.22. Figure 6.20 shows the experimental results for line current regulation and current

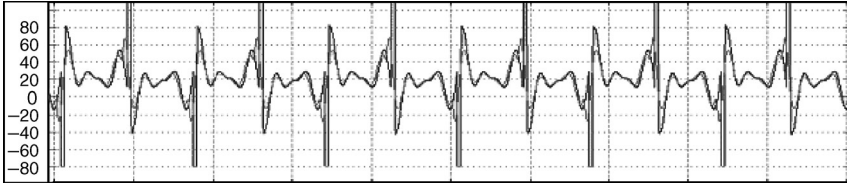


FIGURE 6.12

Voltage of the single-phase series active filter based on the actual method and GSSA method.

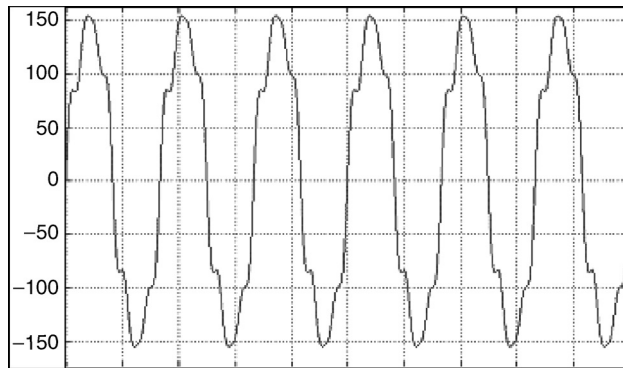


FIGURE 6.13

Source voltage (V_s).

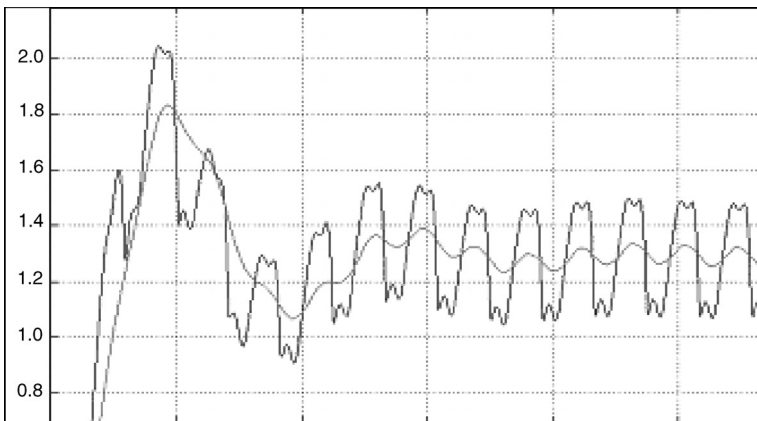


FIGURE 6.14

Output current (i_o).

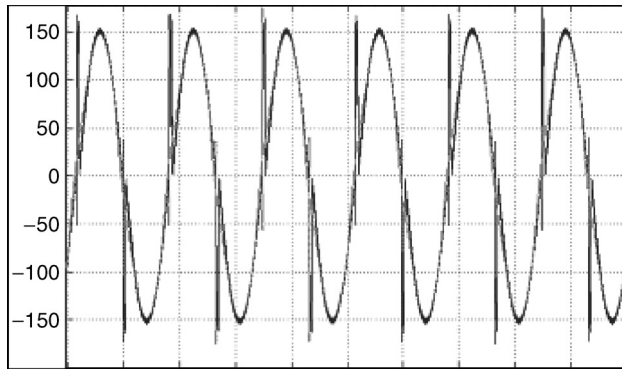


FIGURE 6.15
Load voltages (V_L).

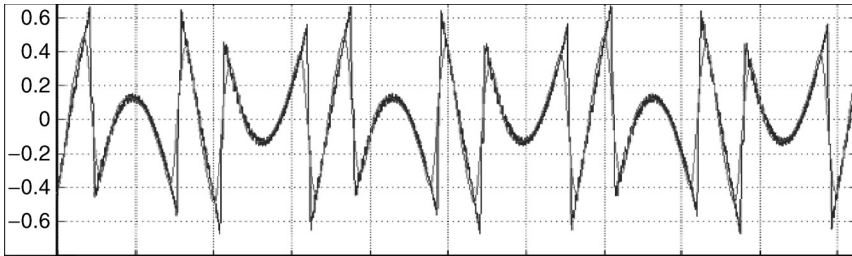


FIGURE 6.16
Phase current of the three-phase shunt active filter based on the actual method and GSSA method.

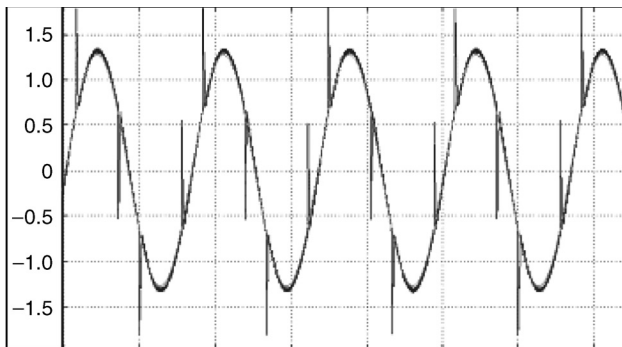


FIGURE 6.17
Source current (i_s).

harmonic cancellation of the single-phase shunt active filter. The results for line voltage regulation and voltage harmonic cancellation of the single-phase series active filter are shown in [Figure 6.21](#). [Figure 6.22](#) shows the experimental results for the three-phase shunt active filter.

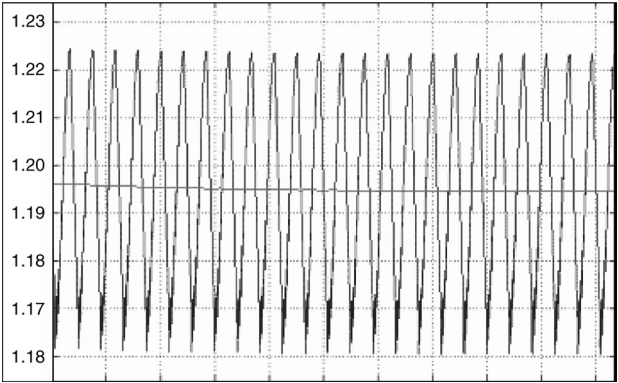


FIGURE 6.18
Output current (i_o).

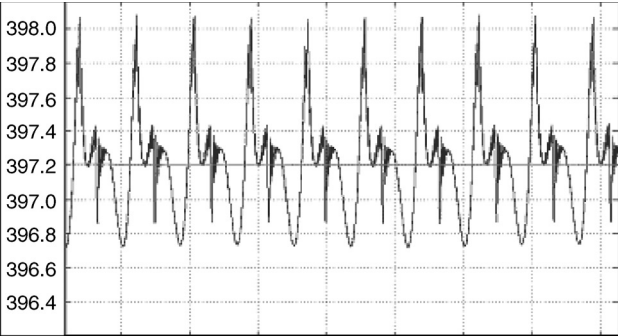


FIGURE 6.19
Capacitor voltages (V_C).

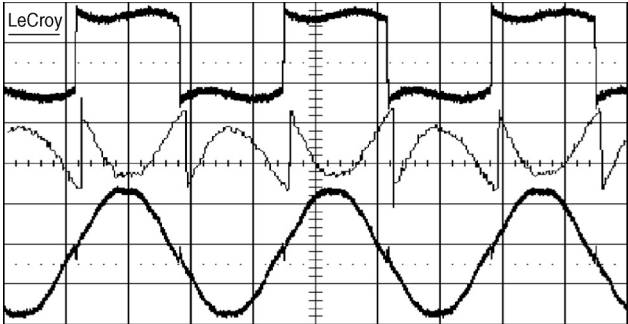
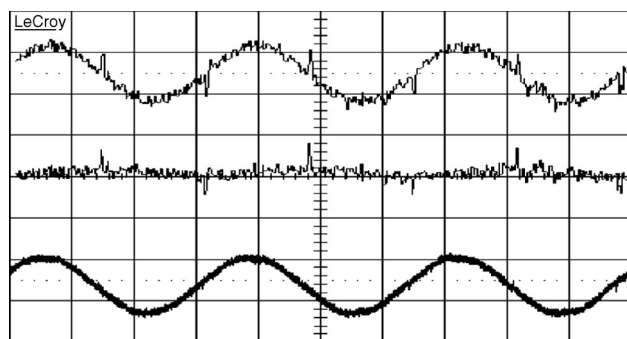
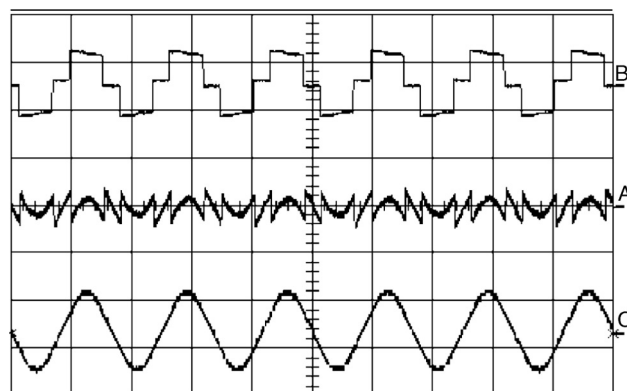


FIGURE 6.20
Experimental results of a single-phase shunt active filter, from top to bottom: current of line, active filter, and load.

**FIGURE 6.21**

Experimental results of a single-phase series active filter, from top to bottom: voltage of line, series converter, and load.

**FIGURE 6.22**

Experimental results, from top to bottom: current of load, parallel converter, and line.

6.2 Digital Control

In this section, a full digital deadbeat controller for active filters and uninterruptible power supply (UPS) systems are presented. First, we discuss the deadbeat control of a simplified single-phase shunt active filter. Theoretically, the controller adjusts the line current and load voltage with two and four sampling periods delay, respectively. In practice, the controller's dynamic is not a pure delay and causes some deviation from theory. Second, the deadbeat control technique is explained for a single-phase series-parallel UPS system. Mathematical analysis of the controller in different operating modes is also explained. In addition, simulation and experimental results are presented to help understand the theoretical description of the system.

6.2.1 Deadbeat Control Technique for a Single-Phase Shunt Active Filter

The configuration of a typical simplified single-phase shunt active filter is shown in Figure 6.23. The state space equation for this system is as follows:

$$L_1 \frac{dI_F}{dt} = V_P - V_S \quad (6.41)$$

Converting this differential equation into a difference equation with a sampling time of T , we have

$$L_1 \frac{I_F(k+1) - I_F(k)}{T} = V_P(k) - V_S(k) \quad (6.42)$$

$$I_F(k+1) - I_F(k) + \frac{T}{L_1} [V_P(k) - V_S(k)] \quad (6.43)$$

If V_S and I_F^* are considered constant over the next period, the output voltage of converter, which corrects the error of I_F after two sampling periods, is as follows [6]:

$$V_P(k+1) = V_S(k+1) + \frac{L_1}{T} [i_F^*(k+1) - i_F(k+1)] \quad (6.44)$$

Substituting Equation 6.43 into Equation 6.44 and updating the reference current for I_F in every two sampling periods, we have

$$V_P(k+1) = \frac{L_1}{T} [i_F^*(k) - i_F(k)] - V_P(k) + V_S(k) + V_S(k+1) \quad (6.45)$$

V_S is considered to be known at all times. Therefore, $V_P(k+1)$ can be calculated easily from the above equation. This equation ensures that the current

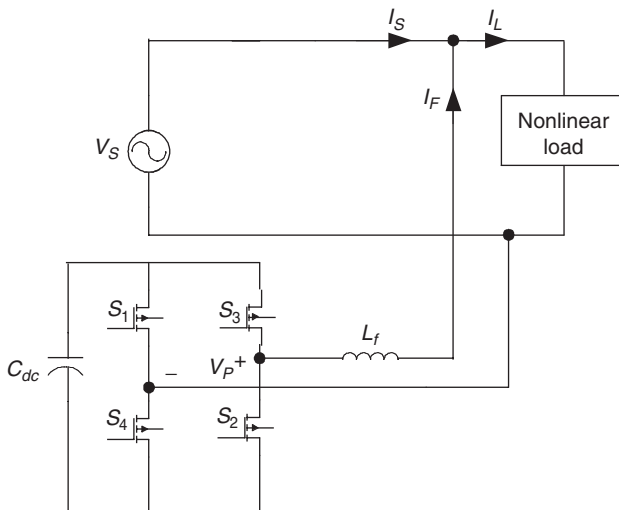
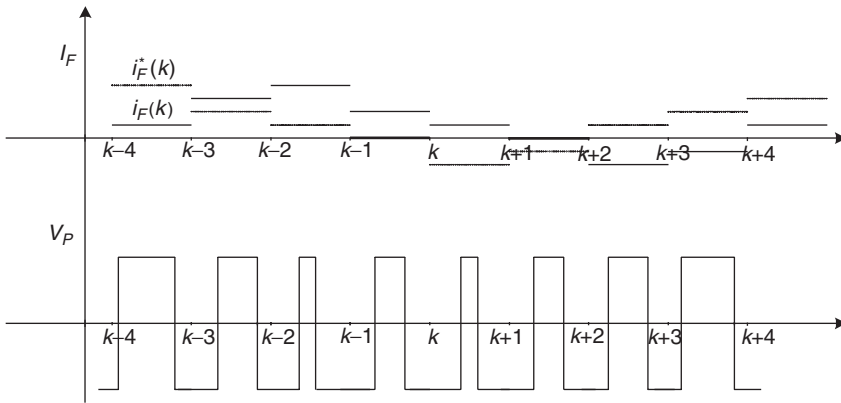


FIGURE 6.23

A typical simplified single-phase shunt active filter.

**FIGURE 6.24**

The timing diagram of I_F and V_P for the simplified shunt active filter.

error between I_F and I_F^* at time $k+2$ goes to zero. The timing diagram of I_F and V_P is shown in Figure 6.24.

6.2.2 Deadbeat Control Technique for Series–Parallel UPS System

The operation of a series–parallel UPS system was discussed in the last chapter and by Bekiarov and Emadi; Rathmann and Warner; Jeon and Cho; Kamran and Habetler; and Da Silva et al. [8–12]. The UPS system has two operating modes: bypass mode and backup mode. The state space equation of the system is different in the bypass and backup mode. During the bypass mode, when the AC line is within the preset tolerance, most of the power is supplied directly from the AC line to the load. Only a small portion of the total power, usually less than 20%, flows through both series and parallel converters. This power is needed to compensate for any difference between the input and output voltages and for power factor correction. At the same time, the parallel inverter charges the battery bank.

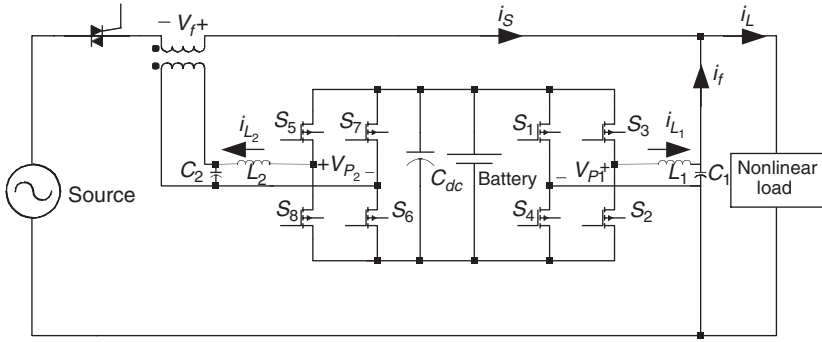
In the backup mode, when the input voltage is beyond a preset tolerance, the static switch trips off the main AC power supply and the parallel converter draws power from the battery bank acting as a conventional DC/AC inverter supplying the load with uninterrupted power. In this mode, the reference voltage is the output of the single-phase PLL, which is freewheeling at 60 Hz. The voltage and current control of both converters in the bypass and backup modes are discussed below.

6.2.2.1 System Equations

The state space equation of the system of Figure 6.25 in bypass mode and continuous time domain is as follows:

$$C_2 \frac{dV_F}{dt} = i_{L_2} - i_s \quad (6.46)$$

$$L_2 \frac{di_{L_2}}{dt} = V_{P_2} - V_F \quad (6.47)$$

**FIGURE 6.25**

A series-parallel UPS topology based on two full-bridge bidirectional converters.

$$C_1 \frac{dV_L}{dt} = i_{L1} - i_F \quad (6.48)$$

$$L_1 \frac{di_{L1}}{dt} = V_{P1} - V_L \quad (6.49)$$

Equations 6.46 and 6.47 correspond to the series converter and Equations 6.48 and 6.49 correspond to the parallel converter. Considering V_F and i_{L2} as state variables for the series converter, we have

$$\begin{bmatrix} V_F \\ i_{L2} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_2 \\ -1/L_2 & 0 \end{bmatrix} \begin{bmatrix} V_F \\ i_{L2} \end{bmatrix} + \begin{bmatrix} 0 \\ 1/L_2 \end{bmatrix} V_{P2} + \begin{bmatrix} -1/C_2 \\ 0 \end{bmatrix} i_s \quad (6.50)$$

V_{P2} and i_s are considered as input and disturbance, respectively. We convert these state space equations into the discontinuous time domain with a sampling period of T_s .

$$\begin{bmatrix} V_F(k+1) \\ i_{L2}(k+1) \end{bmatrix} = \begin{bmatrix} \cos \omega_{02} T_s & \frac{\sin \omega_{02} T_s}{\omega_{02} L_2} \\ -\frac{\sin \omega_{02} T_s}{\omega_{02} L_2} & \cos \omega_{02} T_s \end{bmatrix} \begin{bmatrix} V_F(k) \\ i_{L2}(k) \end{bmatrix} + \begin{bmatrix} \frac{1 - \cos \omega_{02} T_s}{\omega_{02} L_2} \sin \omega_{01} T_s \\ \frac{1}{\omega_{02} L_2} \sin \omega_{01} T_s \end{bmatrix} V_{P2}(k) + \begin{bmatrix} -\frac{1}{\omega_{02} L_2} \sin \omega_{01} T_s \\ 1 - \cos \omega_{02} T_s \end{bmatrix} i_s(k) \quad (6.51)$$

where ω_{02} is the angular resonance frequency of L_2 and C_2 . We consider the sampling frequency of the system much higher than the resonance frequency of L_2 and C_2 . With this assumption, Equation 6.50 is simplified to Equation 6.51.

$$\begin{bmatrix} V_F(k+1) \\ i_{L2}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & T_s \\ -T_s & 1 \end{bmatrix} \begin{bmatrix} V_F(k) \\ i_{L2}(k) \end{bmatrix} + \begin{bmatrix} 0 \\ T_s/L_2 \end{bmatrix} V_{P2}(k) + \begin{bmatrix} -T_s/C_2 \\ 0 \end{bmatrix} i_s(k) \quad (6.52)$$

This conversion is valid for almost $f_s \geq 25f_{02}$.

Considering V_L and i_{L_1} as state variables, the state space equation of the system in the backup mode is as Equation 6.52.

$$\begin{bmatrix} V_L \\ i_{L_1} \end{bmatrix}^* = \begin{bmatrix} 0 & 1/C_1 \\ -1/L_1 & 0 \end{bmatrix} \begin{bmatrix} V_L \\ i_{L_1} \end{bmatrix} + \begin{bmatrix} 0 \\ 1/L_1 \end{bmatrix} V_{P_1} + \begin{bmatrix} -1/C_1 \\ 0 \end{bmatrix} i_L \quad (6.53)$$

With the same method as mentioned above, the discontinuous time-domain equations with a sampling period of T_s are achieved as follows:

$$\begin{bmatrix} V_L(k+1) \\ i_{L_1}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & T_s \\ -T_s & 1 \end{bmatrix} \begin{bmatrix} V_L(k) \\ i_{L_1}(k) \end{bmatrix} + \begin{bmatrix} 0 \\ T_s/L_1 \end{bmatrix} V_{P_1}(k) + \begin{bmatrix} -T_s/C_1 \\ 0 \end{bmatrix} i_L(k) \quad (6.54)$$

This conversion is valid for $f_s \gg f_{0_1}$, where f_{0_1} is the resonant frequency of L_1 and C_1 .

6.2.2.2 Series Converter

The current equation according to Equation 6.52 is as follows:

$$i_{L_2}(k+1) = i_{L_2}(k) + \frac{T_s}{L_2} [V_{P_2}(k) - V_F(k)] \quad (6.55)$$

Alternatively, this equation can be obtained by converting Equation 6.47 from a differential equation to a difference equation. The same suggestion of $f_s \gg 25f_0$ has to be made for this conversion. If V_F and $i_{L_2}^*$ are considered constant over the next period, the output voltage of the series converter, which corrects the error of i_{L_2} after two sampling periods, is as follows [13]:

$$V_{P_2}(k+1) = V_F(k+1) + \frac{L_2}{T_s} [i_{L_2}^*(k+1) - i_{L_2}(k+1)] \quad (6.56)$$

$V_F(k+1)$ can be linearly estimated from the previous values as follows:

$$V_F(k+1) = V_F(k) + [V_F(k) - V_F(k-1)] = 2V_F(k) - V_F(k-1) \quad (6.57)$$

Substituting Equation 6.55 and 6.57 into Equation 6.56 and updating the reference current for i_{L_2} in every two sampling periods, we have

$$V_{P_2}(k+1) = \frac{L_2}{T_s} [i_{L_2}^*(k) - i_{L_2}(k)] - V_{P_2}(k) + 3V_F(k) - V_F(k-1) \quad (6.58)$$

Equation 6.58 ensures that the current error between i_{L_2} and $i_{L_2}^*$ at time $k+2$ goes to zero.

Avoiding interaction between voltage and current control loops, the output voltage of the series converter, V_F , is sampled at half of the current sampling frequency. The voltage equation according to Equation 6.52 is as follows:

$$V_F(k+1) = V_F(k) + \frac{T_s}{C_2} i_{C_2}(k) \quad (6.59)$$

$$V_F(k+2) = V_F(k+1) + \frac{T_s}{C_2} i_{C_2}(k+1) = V_F(k) + \frac{T_s}{C_2} i_{C_2}(k) + \frac{T_s}{C_2} i_{C_2}(k+1) \quad (6.60)$$

As current control is suggested to be deadbeat with a delay of two sampling periods, we have

$$i_{C_2}(k) = i_{C_2}^*(k-2), \quad i_{C_2}(k) = i_{C_2}^*(k-1) \quad (6.61)$$

Substituting Equation 6.59 into Equation 6.58 and updating the reference current at every two sampling frequencies, we obtain

$$V_F(k+2) = V_F(k) + \frac{2T_s}{C_2} i_{C_2}^*(k-2) \quad (6.62)$$

The current of $i_{C_2}^*$ at time k , corrects the voltage error of V_F at time $k+4$, is as follows:

$$i_{C_2}^*(k) = \frac{C_2}{2T_s} [V_F^*(k) - V_F(k)] - i_{C_2}^*(k-2) \quad (6.63)$$

A block diagram of implementation of current and voltage control system in the bypass mode is shown in Figure 6.26.

6.2.2.3 Parallel Converter

If the sampling frequency is considered much higher than the resonance frequency of C_1 and L_1 , Equation 6.49 can be converted from a differential equation to a difference equation as follows:

$$i_{L_1}(k+1) = i_{L_1}(k) + \frac{T_s}{L_1} [V_{P_1}(k) - V_L(k)] \quad (6.64)$$

This equation is the same as Equation 6.55, and the control algorithm ensuring deadbeat control can be achieved as follows:

$$V_{P_1}(k+1) = \frac{L_1}{T_s} [i_{L_1}^*(k) - i_{L_1}(k)] - V_{P_1}(k) + 3V_L(k) - V_L(k-1) \quad (6.65)$$

$$i_{L_1}^*(k) = I_F^*(k) + i_{C_1}(k) \quad (6.66)$$

$i_{C_1}(k)$ is easily calculated from the current and previous values of V_L . The block diagram of the implementation of the current control of the parallel

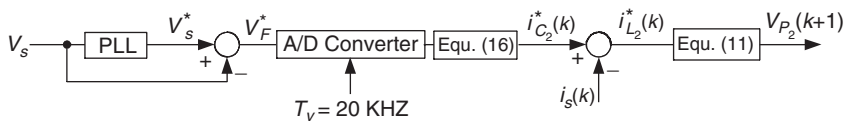
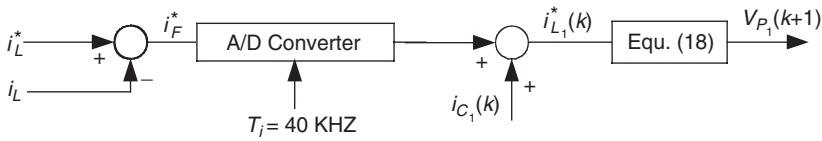
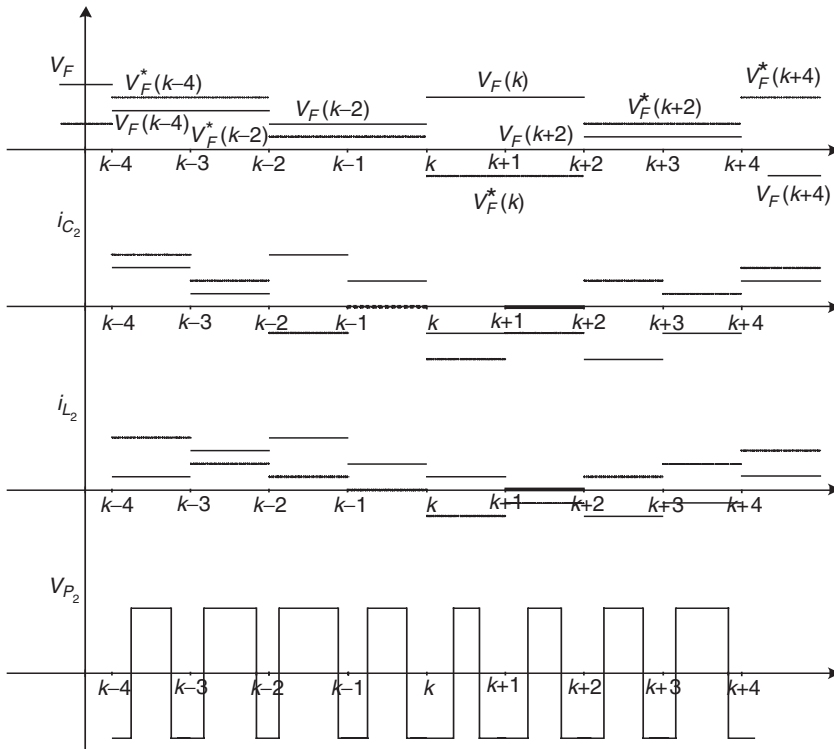


FIGURE 6.26

Implementation of the current and voltage control of the series converter in the bypass mode.

**FIGURE 6.27**

Implementation of the current control of the parallel converter in the bypass mode.

**FIGURE 6.28**

Timing of the current and voltage controller, from top to bottom: output of series converter, current of C_2 , output current of parallel converter, and output voltage of series converter.

converter is shown in Figure 6.27. The timing of the control system in the bypass mode is shown in Figure 6.28.

6.2.2.4 Control of a Parallel Converter in Backup Mode

The current equation according to Equation 6.54 is as follows:

$$i_{L_1}(k+1) = i_{L_1}(k) + \frac{T_s}{L_1} [V_{P_1}(k) - V_L(k)] \quad (6.67)$$

Accordingly, considering V_L and $i_{L_1}^*$ constant over the next period, the output voltage of the parallel converter, which corrects the error of i_{L_1} after two sampling periods, is as follows [13]:

$$V_{P_1}(k+1) = V_L(k+1) \frac{L_2}{T_s} [i_{L_1}^*(k+1) - i_{L_1}(k+1)] \quad (6.68)$$

$V_L(k+1)$ is linearly estimated from previous values as follows:

$$V_L(k+1) = V_L(k) + [V_L(k) - V_L(k-1)] = 2V_L(k) - V_L(k-1) \quad (6.69)$$

Substituting Equations 6.69 and 6.67 into Equation 6.68 and updating reference current for i_{L_1} in every two sampling periods, we have

$$V_{P_1}(k+1) = \frac{L_1}{T_s} [i_{L_1}^*(k) - i_{L_1}(k)] - V_{P_1}(k) + 3V_L(k) - V_L(k-1) \quad (6.70)$$

Equation 6.70 ensures that the current error between i_{L_1} and $i_{L_1}^*$ at time $k+2$ goes to zero.

Correspondingly, load voltage, V_L , is sampled at half of the current sampling frequency. The voltage equation according to Equation 6.54 is as follows:

$$V_L(k+1) = V_L(k) + \frac{T_s}{C_1} i_{C_1}(k) \quad (6.71)$$

$$V_L(k+2) = V_L(k+1) + \frac{T_s}{C_1} i_{C_1}(k+1) = V_L(k) + \frac{T_s}{C_1} i_{C_1}(k) + \frac{T_s}{C_1} i_{C_1}(k+1) \quad (6.72)$$

As current control is suggested to be deadbeat with a delay of two sampling periods, we have

$$i_{C_1}(k) = i_{C_1}^*(k-2), \quad i_{C_1}(k+1) = i_{C_1}^*(k-1) \quad (6.73)$$

Substituting Equation 6.73 into Equation 6.72 and updating the reference current at every two sampling frequencies, we obtain

$$V_L(k+2) = V_L(k) + \frac{2T_s}{C_1} i_{C_1}^*(k-2) \quad (6.74)$$

The current of $i_{C_1}^*$ at time k , which corrects the voltage error of V_L at time $k+4$, is as follows:

$$i_{C_1}^*(k) = \frac{C_1}{2T_s} [V_L^*(k) - V_L(k)] - i_{C_1}^*(k-2) \quad (6.75)$$

6.2.3 Digital Controller Implementation

The whole digital control system can be built in a TMS320LF2407A digital signal processor (DSP). This DSP provides 40 MHz clock frequency, 40 MIPS, 2.5K RAM, and 32K flash memory. Source voltage, reference voltage, and

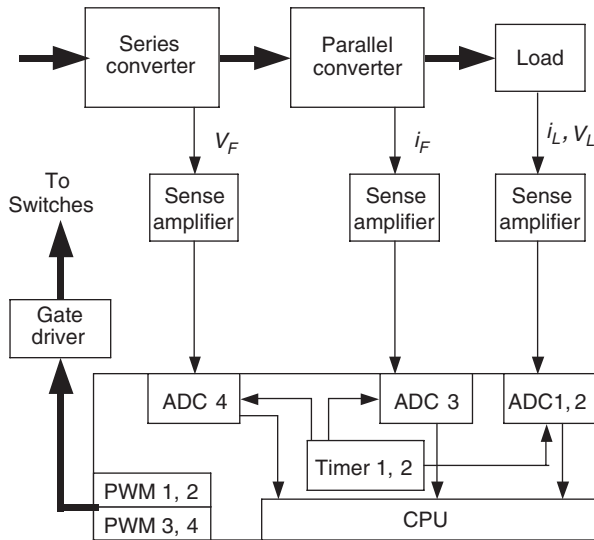


FIGURE 6.29
Block diagram of PWM output implementation.

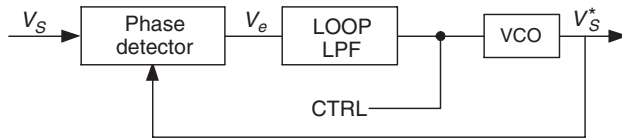


FIGURE 6.30
Block diagram of the single-phase PLL.

load voltage are sampled using 16 available internal A/D converters with a sampling frequency of 20 kHz. Source current and load current are sampled with a 40 kHz sampling frequency. The resolution of A/D converters is 10 bits. Timing for current and voltage controllers is provided by two internal general timers. Pulse width modulation (PWM) outputs for each converter are generated by the DSP using internal 16-bit pulse width modulators. Figure 6.29 shows the simplified block diagram of control system implementation. A phase lock loop system can be made with a simple AD4001 IC. Its block diagram is shown in Figure 6.30.

6.2.4 Analysis of Controller

A block diagram of the current and voltage controller in the bypass mode for the series converter is shown in Figure 6.31. The voltage regulator is a pure deadbeat controller with a delay of two sampling periods, including the time consumed for calculation. G_1 is the time delay needed for calculations and

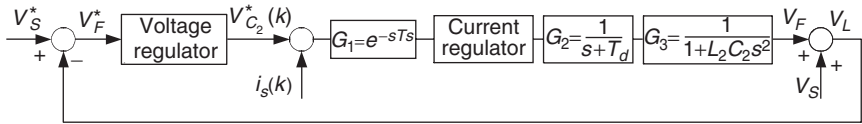


FIGURE 6.31
Block diagram of the current and voltage controller of the series converter in the bypass mode.

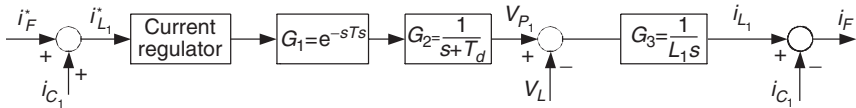


FIGURE 6.32
Current controller of the parallel converter in the bypass mode.

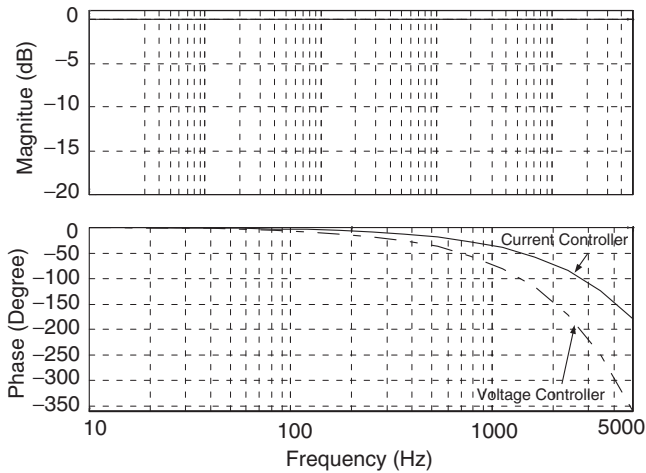
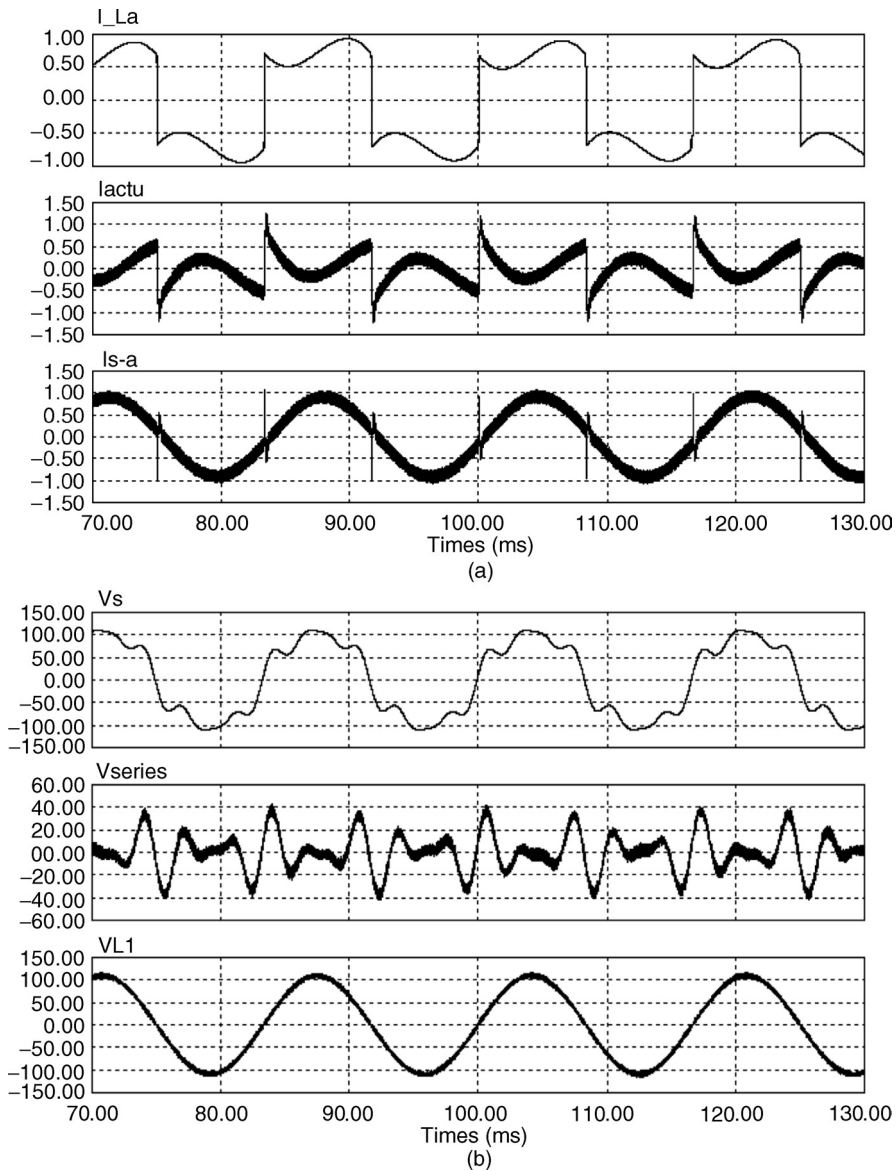


FIGURE 6.33
Frequency response of the current and voltage controller.

analog-to-digital conversions. G_2 is the time delay caused by the PWM inverter and G_3 is the transfer function of the low-pass filter. The current regulator is also considered as a pure delay. The output voltage of the series converter follows its reference with four sampling periods of delay. In practice, the dynamic of the current regulator is not a pure delay and shows some deviation from the deadbeat controller. Therefore, the total settling time is more than 100 μ s. Figure 6.32 shows the current controller of the parallel converter in the bypass mode. The output current of the converter follows its reference with a 50 μ s delay. Figure 6.33 shows the frequency response of the current controller and voltage controller based on the deadbeat control method.

**FIGURE 6.34**

Simulation results of the system in the bypass mode: (a) load, parallel converter, and line current, and (b) line, series converter, and load voltage.

The phase delay of the controller linearly increases with frequency increment. Dislike phase, the gain of the controller remains unity for all frequency ranges. For frequencies lower than 1 kHz, the phase lag of the current controller is negligible. This range includes the major current harmonics up to 15th harmonic. The ability of the controller to cancel current harmonics for

frequencies more than 2 kHz deteriorates. For frequencies more than 5 kHz, the current controller magnifies the current harmonic. For frequencies around 10 kHz, the controller is unstable. In the practical system, the parallel converter in the bypass mode is not designed to cancel current harmonics with frequencies more than 1 kHz. Additionally, the low-pass filter formed by L_1 and C_1 cancels the produced current harmonics of the parallel converter. The phase delay of voltage controller is twice that of the current controller. Therefore, the series converter in the bypass mode is capable of canceling voltage harmonics up to 1 kHz.

Typical simulation and experimental results of the system are shown in Figure 6.34, Figure 6.35, and Figure 6.36. Figure 6.34 shows the simulation results of the system in the bypass mode with PSIM software. The series converter compensates the voltage sag and voltage harmonic of the input AC source. The parallel converter mitigates the current harmonic of load current. To validate the digital deadbeat control method for the single-phase UPS topology, an experimental setup of the system was also built and tested in the lab. Typical parameters of the system are shown in Table 6.1. Load current harmonic mitigation by the parallel converter in the bypass

TABLE 6.1
Typical parameters of the circuit

Nominal values:	
Line voltage	120 Vrms
DC bus voltage	270 V
Nominal system power	650 W
Line frequency	60 Hz
Voltage passive filter:	
L_2	4.9 mH
C_2	5.6 μ F
Cut-off frequency	960 Hz
Current passive filter:	
L_1	2.2 mH
C_1	4.7 μ F
Cut-off frequency	1565 Hz

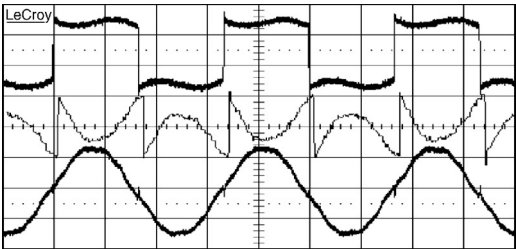
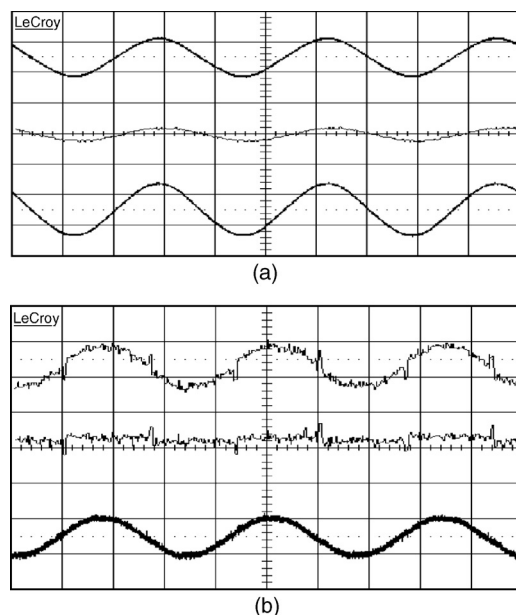


FIGURE 6.35
Experimental results of the UPS system for load current harmonics compensation, from top to bottom: current of load, parallel converter, and line.

**FIGURE 6.36**

Experimental results of the UPS system in the presence of source voltage (a) sag, and (b) harmonics, from top to bottom: voltage of line, series converter, and load.

mode is shown in Figure 6.35. A supply voltage including voltage harmonic and voltage sag was applied to the system. The load is a nonlinear single-phase inductive load. Figure 6.36 shows the compensation of the voltage sag and voltage harmonic by the series converter. The total harmonic distortion (THD) of load voltage is measured to be less than 2%.

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